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(51) INT CL[5]
H03M 3/00

(52) UK CL (Edition M)
H3H HAH H1X
U1S S2105 S2118 S2119 S2175 S2202

(56) Documents Cited
US 5179380 A

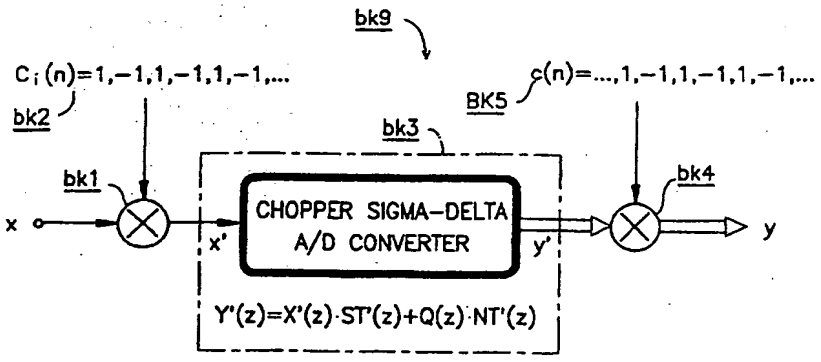
(58) Field of Search
UK CL (Edition L) H3H HAH
INT CL[5] H03M
Online databases:WPI,INSPEC

(54) Chopper-stabilized sigma-delta converter

(57) A chopper-stabilized sigma-delta analog-to-digital converter (ADC) bk9 has a discrete-time multiplier bk1 receiving an analog input signal x and a first discrete-time sequence bk2, and multiplying them to produce a chopped analog signal x'. A chopper sigma-delta ADC bk3 converts the chopped analog signal x' into a digital output signal y'. The chopper sigma-delta ADC is characterized in z-domain by:

$$Y'(z)=X'(z)ST'(z) + Q(z)NT'(z),\ z=e^{jw}$$

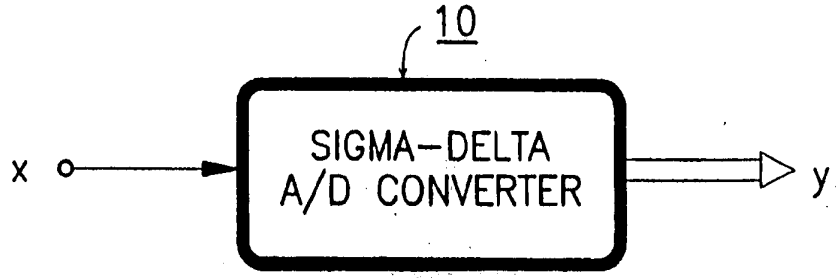
wherein ST'(z) is a signal transfer function, and has a passband in a high-frequency range, and NT'(z) is a noise transfer function having a high attenuation in the high-frequency range. In this way, the circuit low-frequency noises can be removed to increase the resolution of the converter bk9.



$$Y(z)=X(Z)\cdot ST(z)+Q(z)\cdot NT(z),z=e^{j\omega}$$

FIG. 2(a)

GB 2 278 247 A



$$Y(z)=X(Z)\cdot ST(z)+Q(z)\cdot NT(z), z=e^{j\omega}$$

FIG. 1(a)(PRIOR ART)

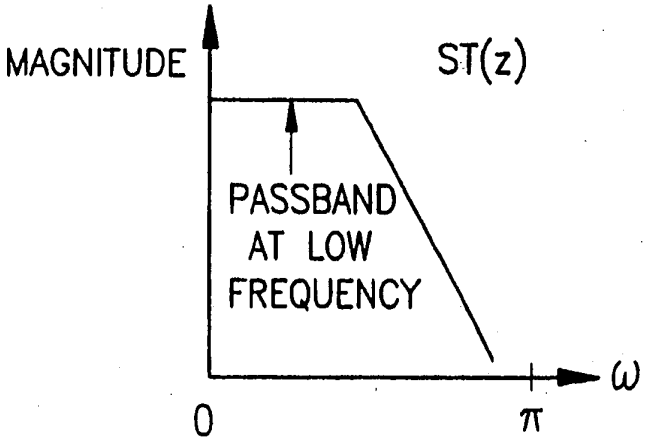


FIG. 1(b)(PRIOR ART)

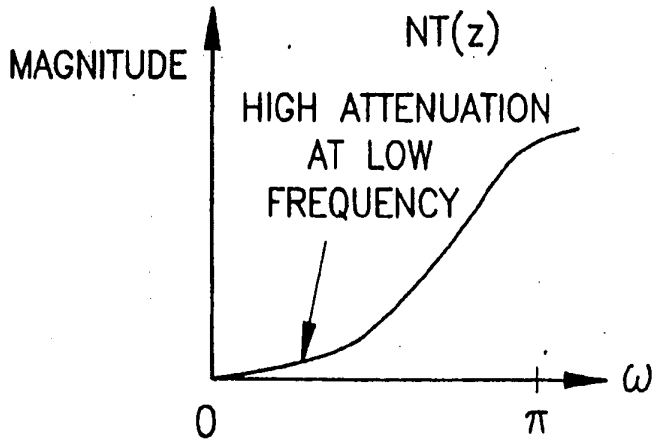


FIG. 1(c)(PRIOR ART)

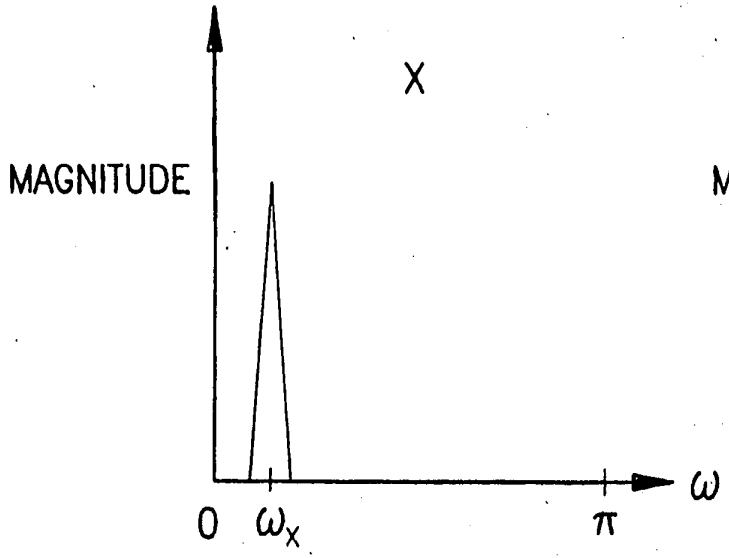


FIG. 1(d)(PRIOR ART)

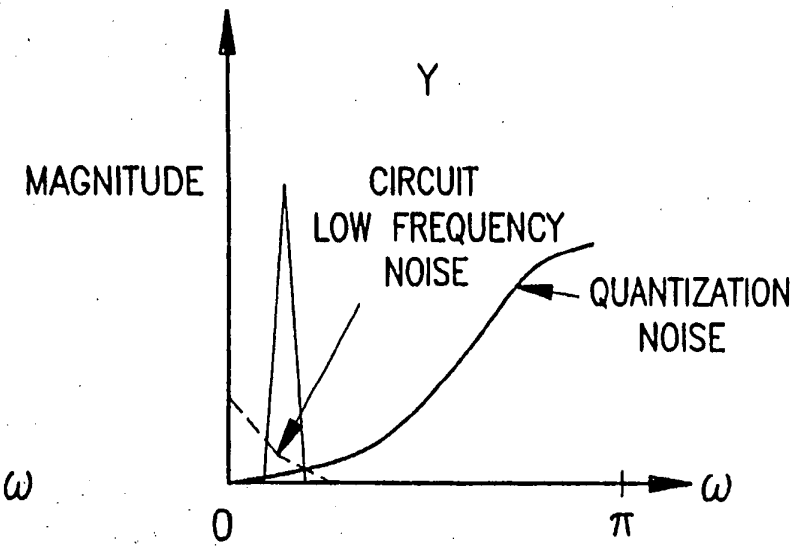
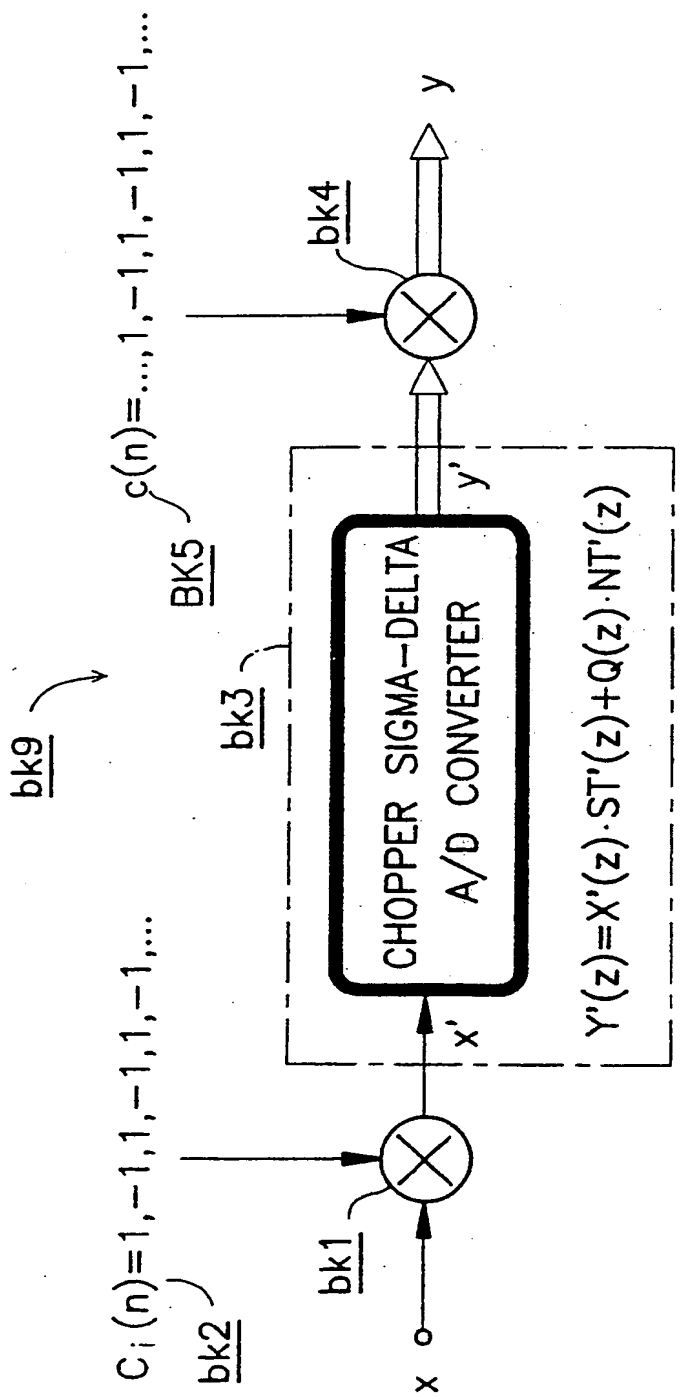
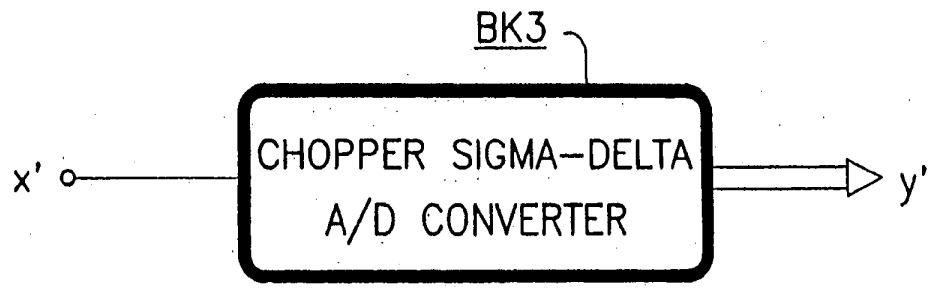


FIG. 1(e)(PRIOR ART)



$$Y(z)=X(Z)\cdot ST(z)+Q(z)\cdot NT(z), z=e^{j\omega}$$

FIG. 2(a)



$$Y'(z)=X'(z)\cdot ST'(z)+Q(z)\cdot NT'(z), z=e^{j\omega}$$

FIG. 2(b)

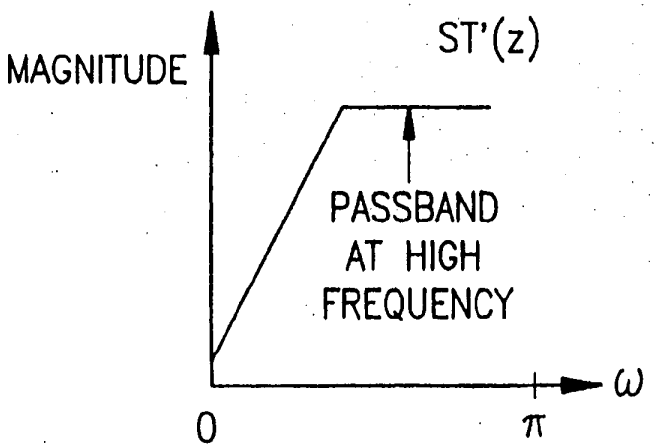


FIG. 2(c)

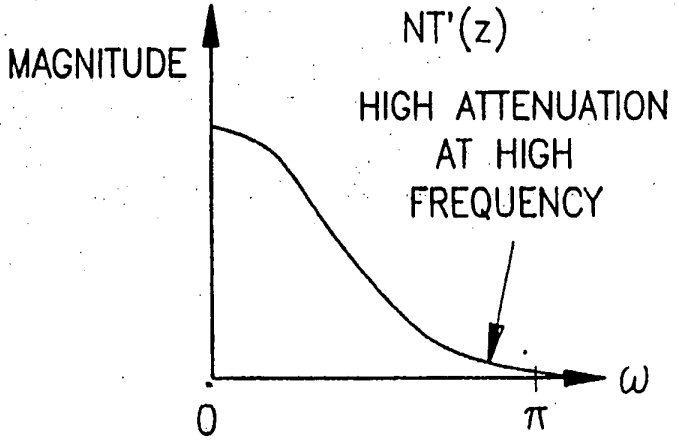


FIG. 2(d)

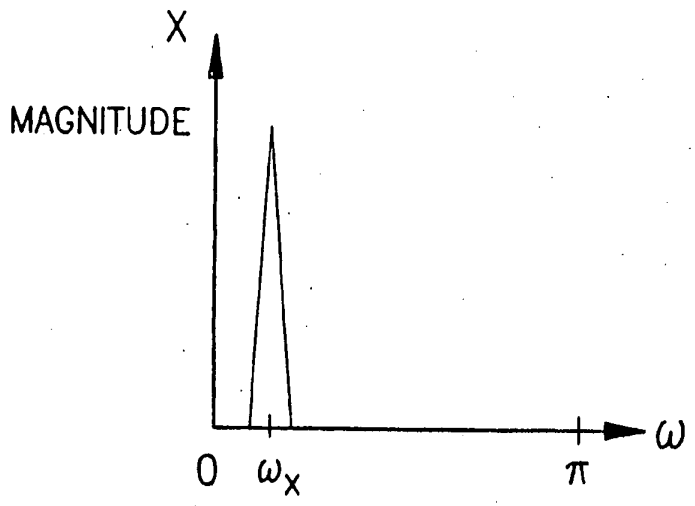


FIG. 2(e)

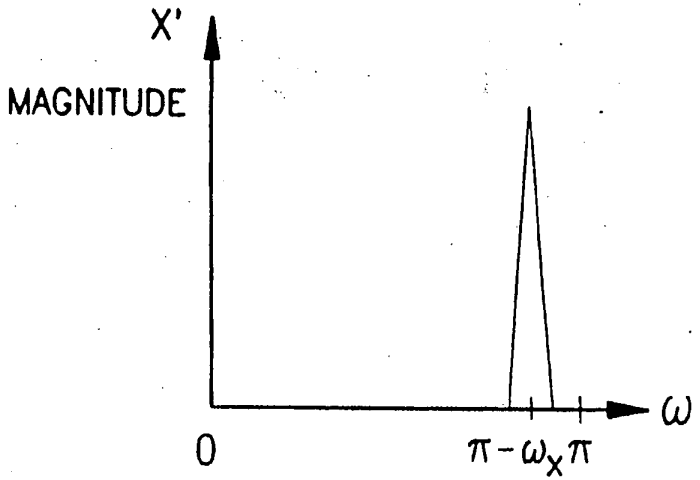


FIG. 2(f)

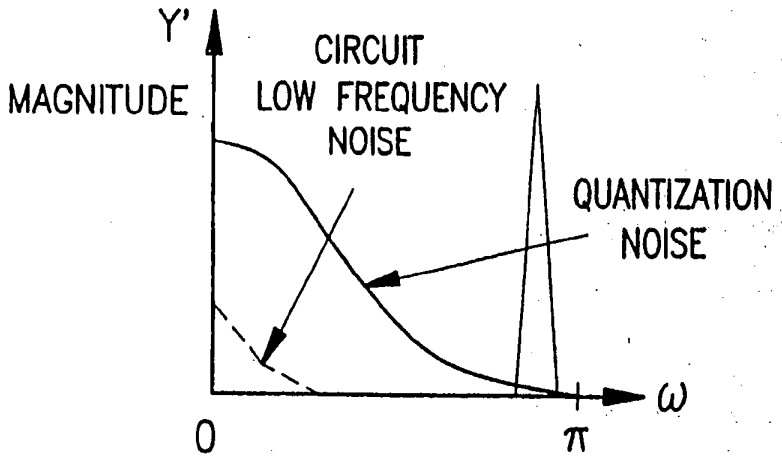


FIG. 2(g)

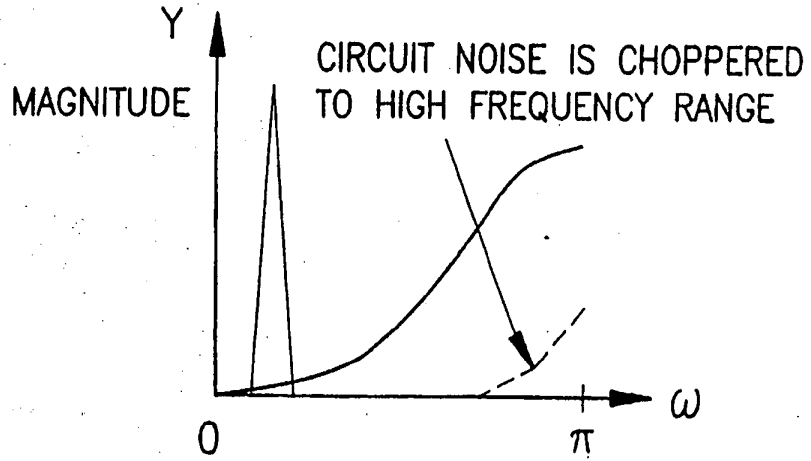
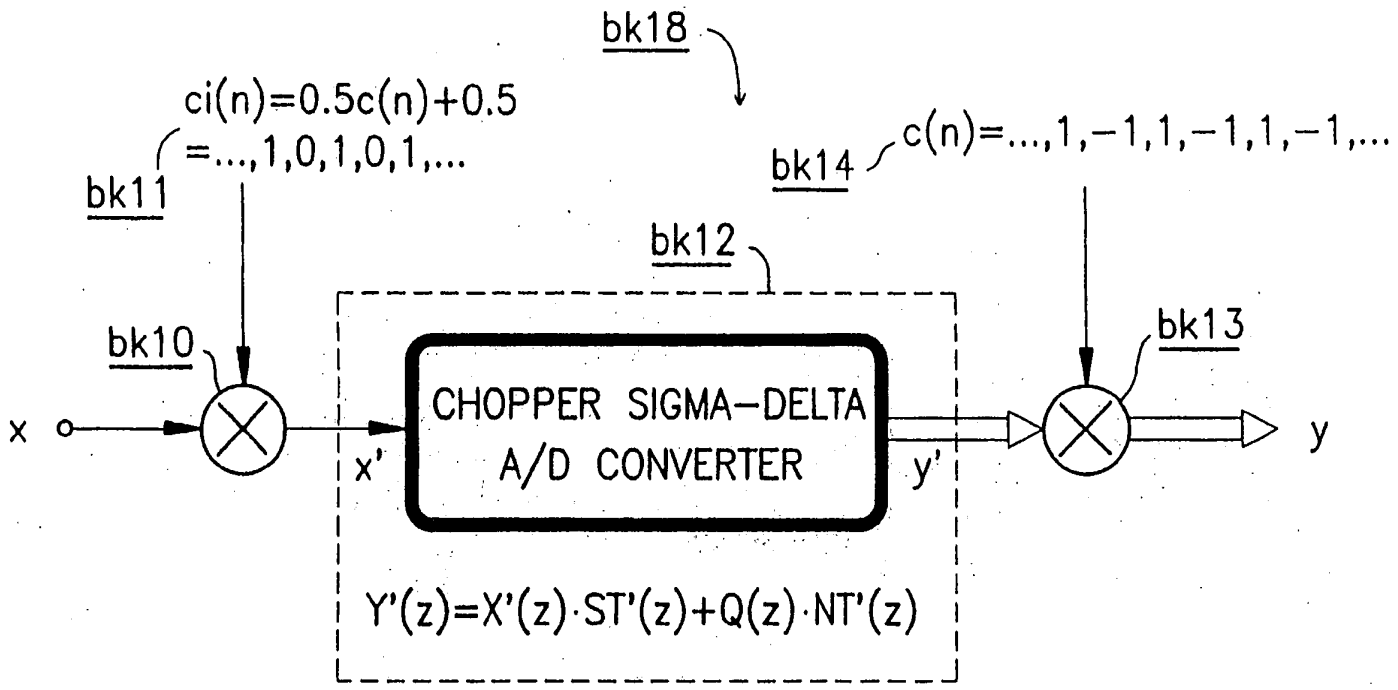
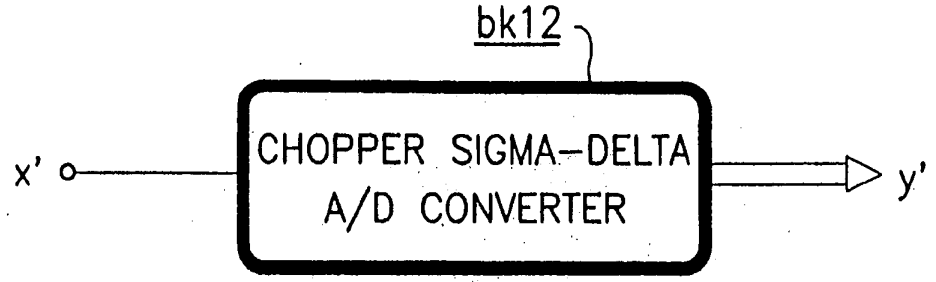


FIG. 2(h)



$$Y(z)=0.5X(z)\cdot ST(z)+Q(z)\cdot NT(z),z=e^{j\omega}$$

FIG. 3(a)



$$Y'(z)=X'(z)\cdot ST'(z)+Q(z)\cdot NT'(z), z=e^{j\omega}$$

FIG. 3(b)

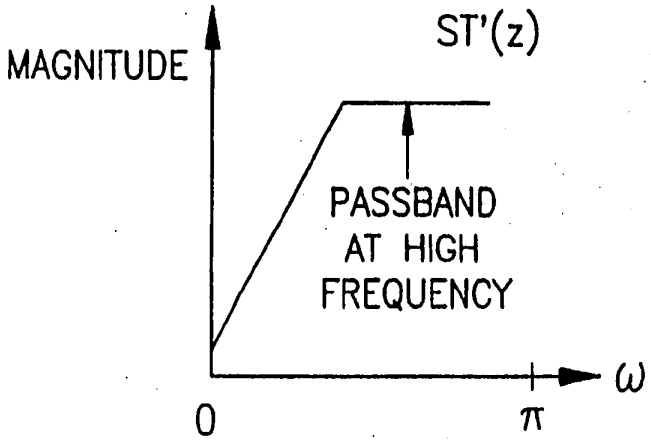


FIG. 3(c)

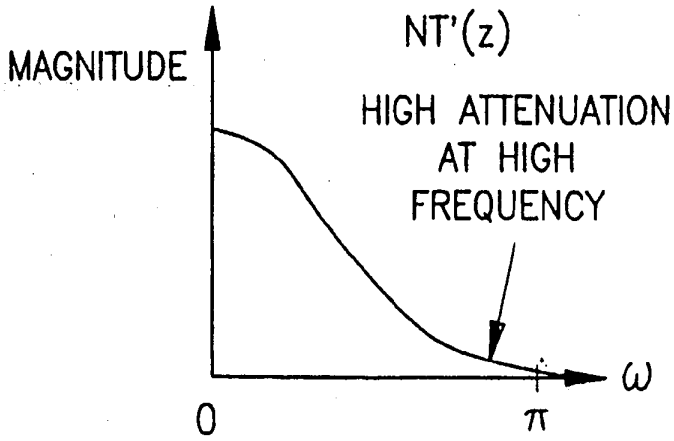


FIG. 3(d)

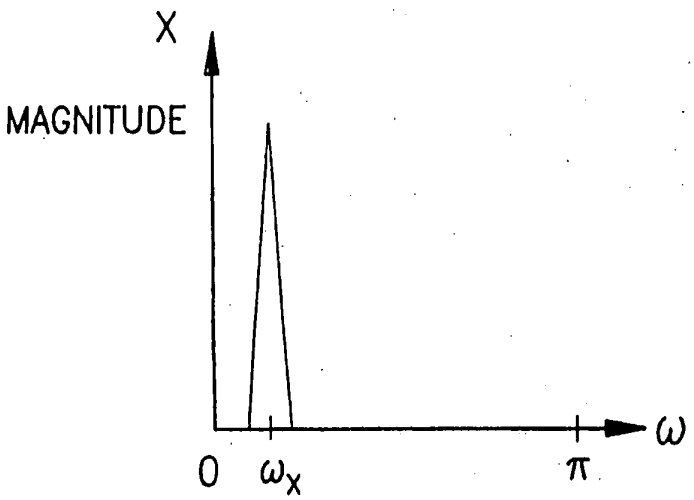


FIG. 3(e)

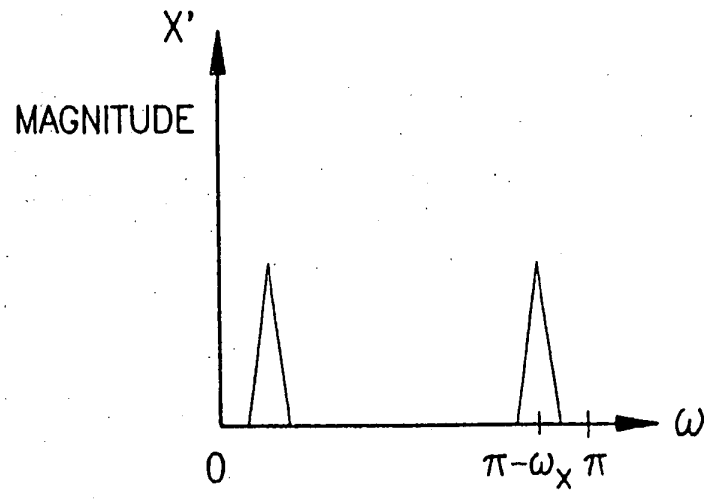


FIG. 3(f)

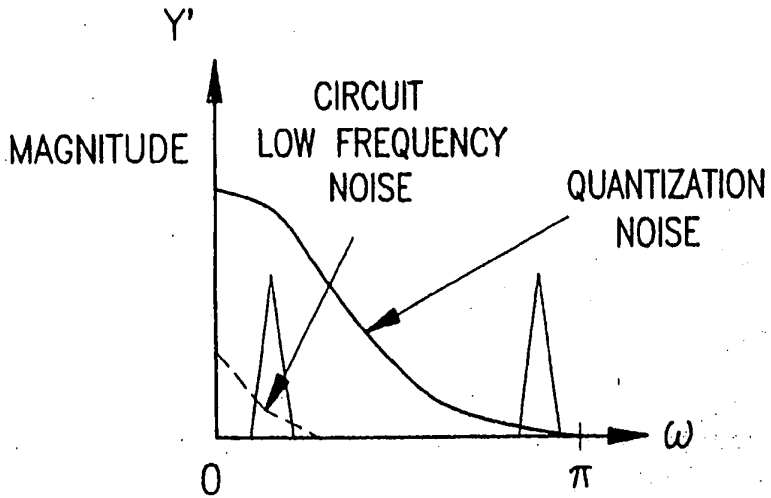


FIG. 3(g)

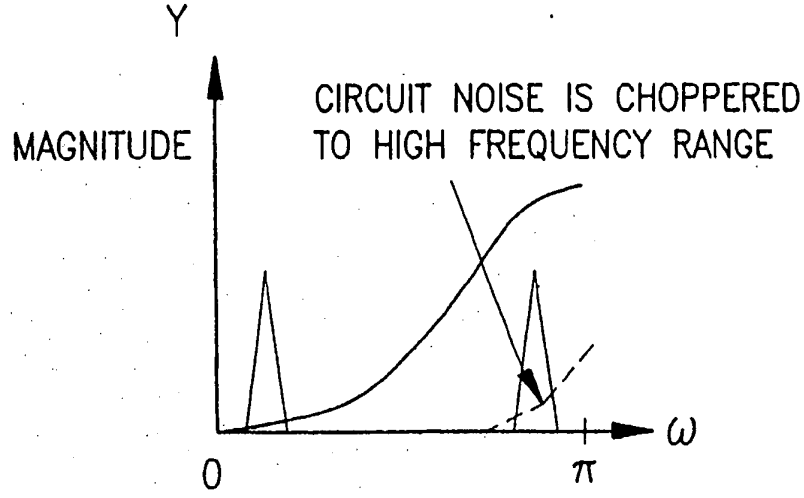


FIG. 3(h)

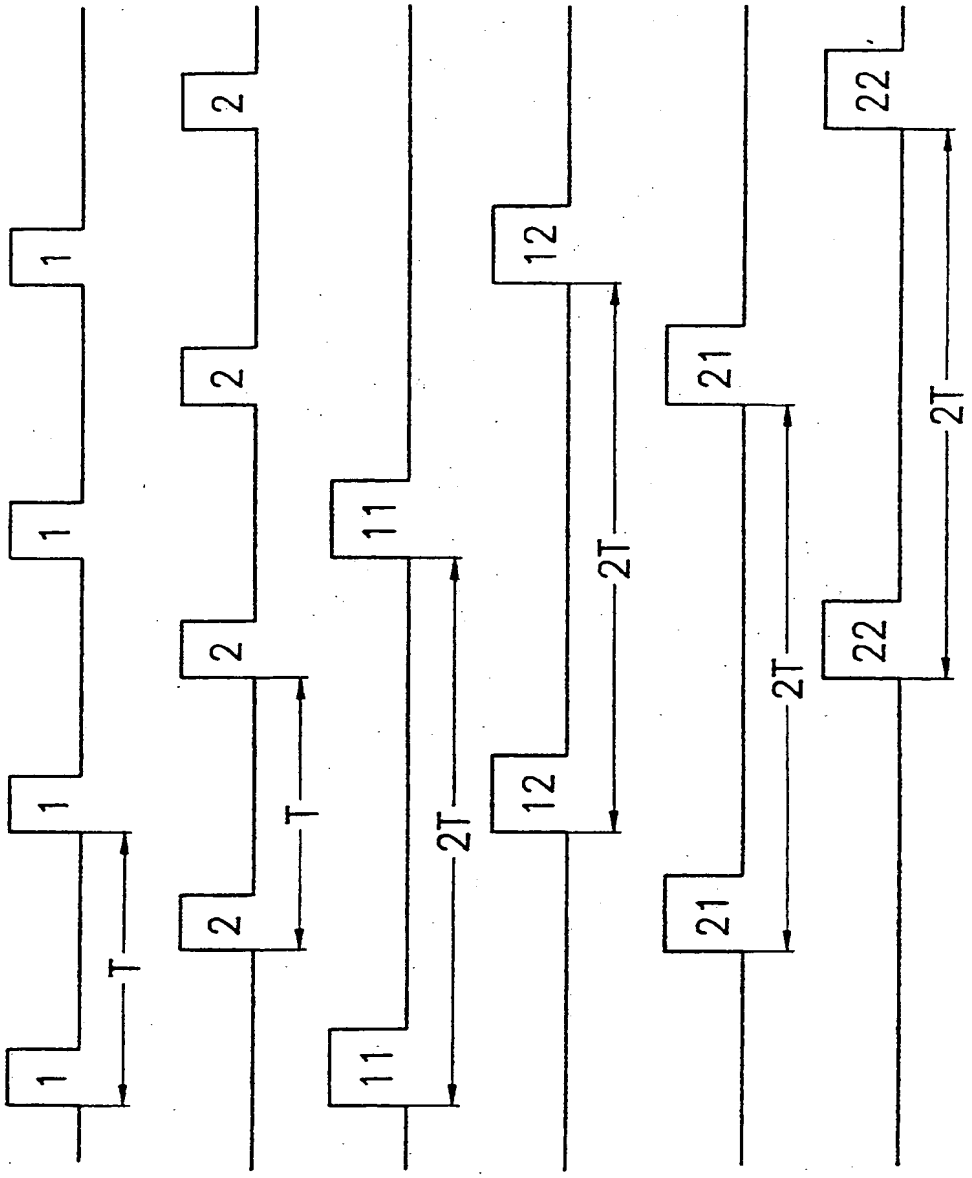


FIG. 4

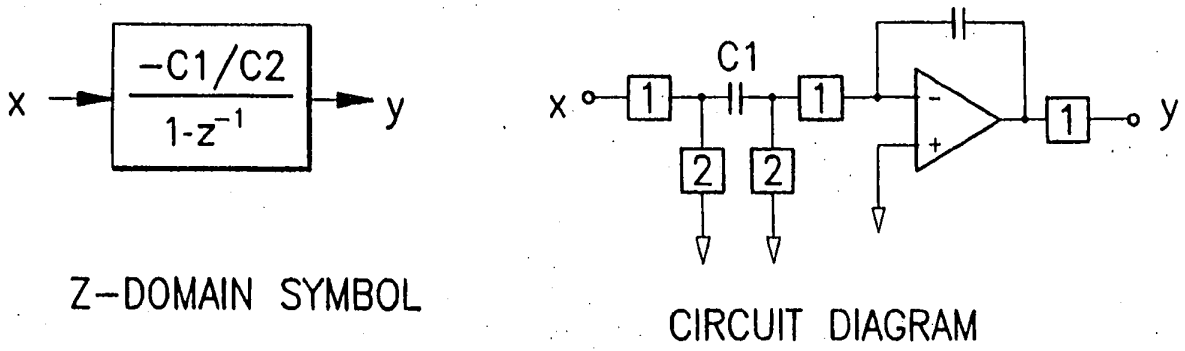

x
-C1/C2
1-z^-1
y
Z-DOMAIN SYMBOL
C2
C1
x
1
1
1
2
2
y
CIRCUIT DIAGRAM

FIG. 5(a)

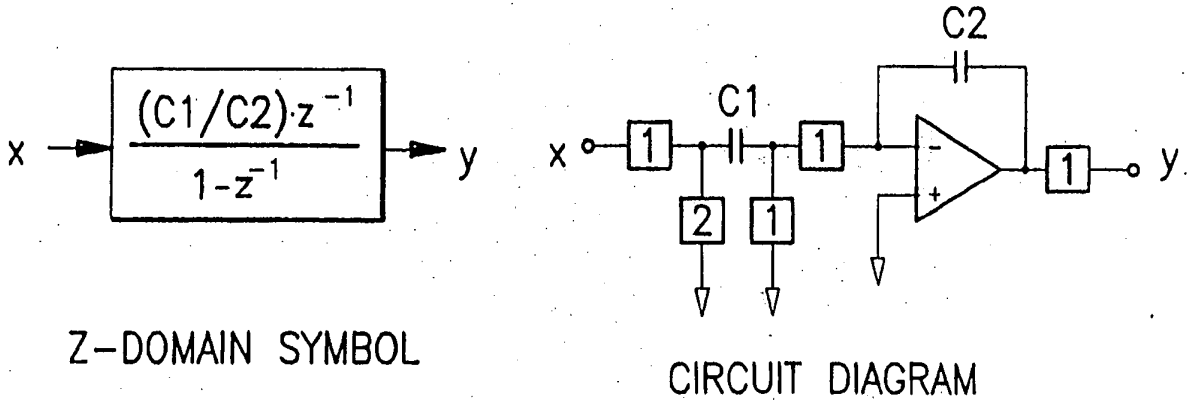
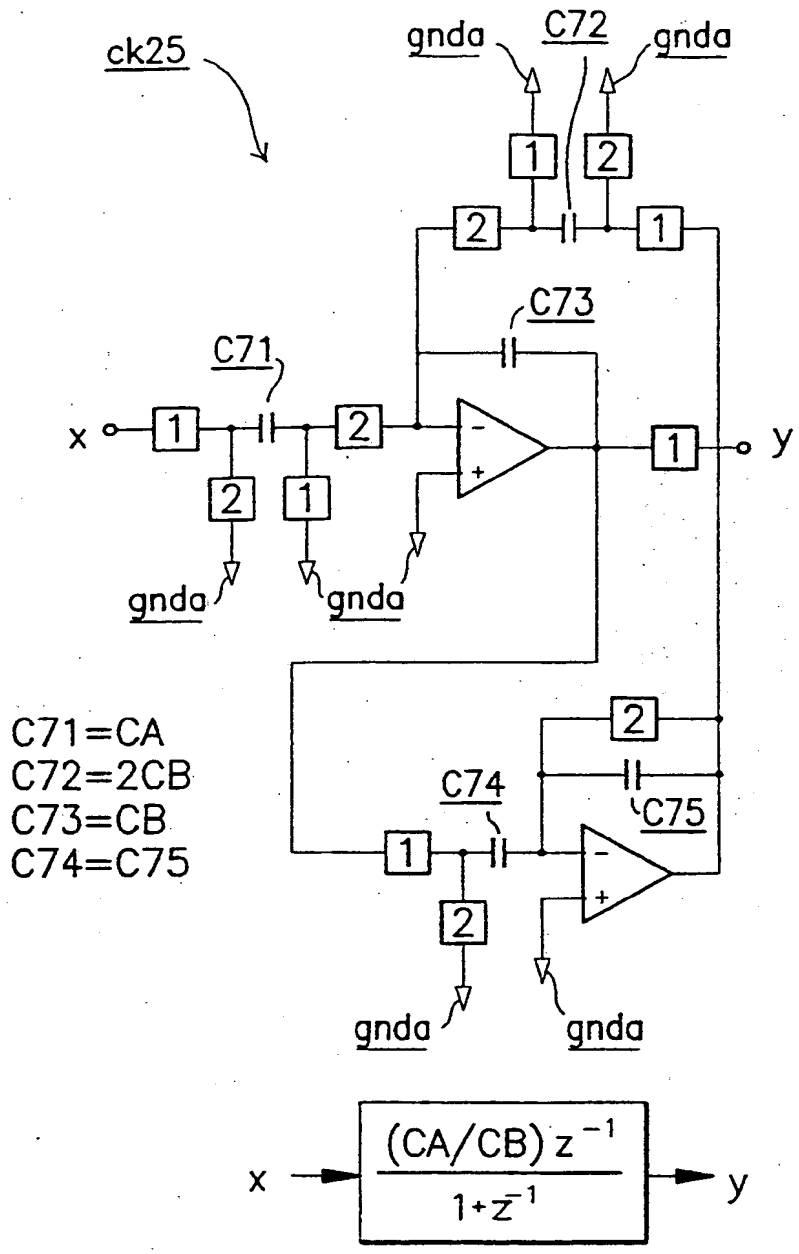
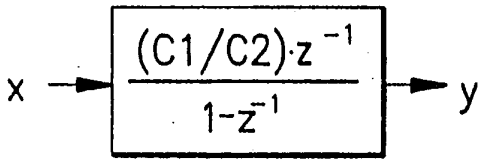

x
(C1/C2)·z^-1
1-z^-1
y
Z-DOMAIN SYMBOL
C2
C1
x
1
1
1
2
1
y
CIRCUIT DIAGRAM

FIG. 5(b)

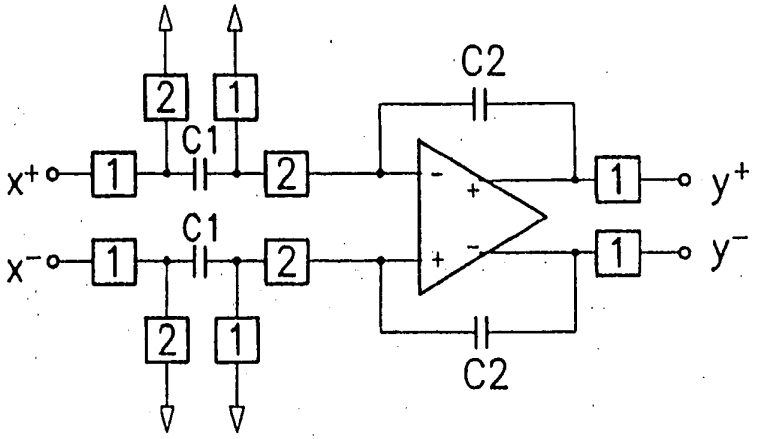


Z-DOMAIN SYMBOL

FIG. 5(c)



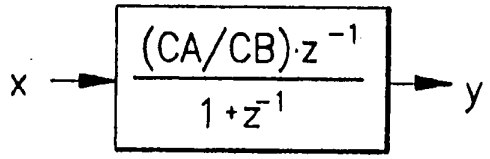
Z-DOMAIN SYMBOL



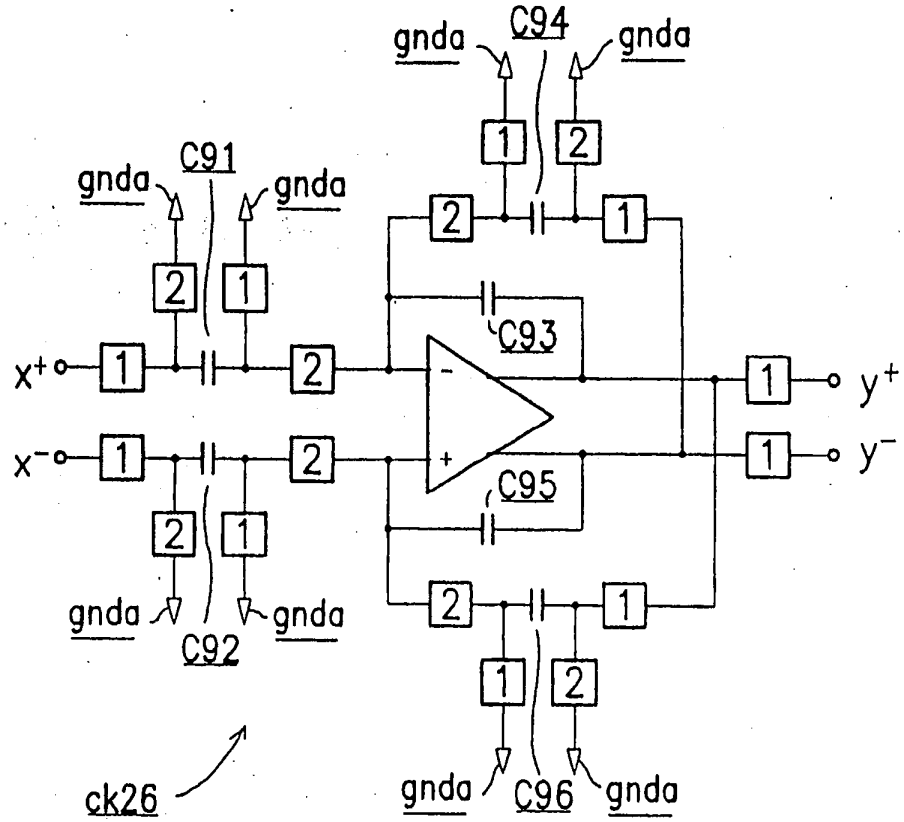
CIRCUIT DIAGRAM

FIG. 6(a)(PRIOR ART)

C91=C92=CA
C93=C95=CB
C94=C96=2CB

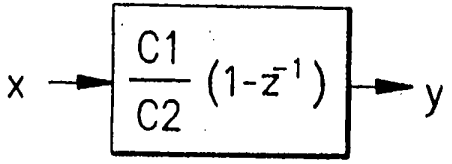


Z-DOMAIN SYMBOL

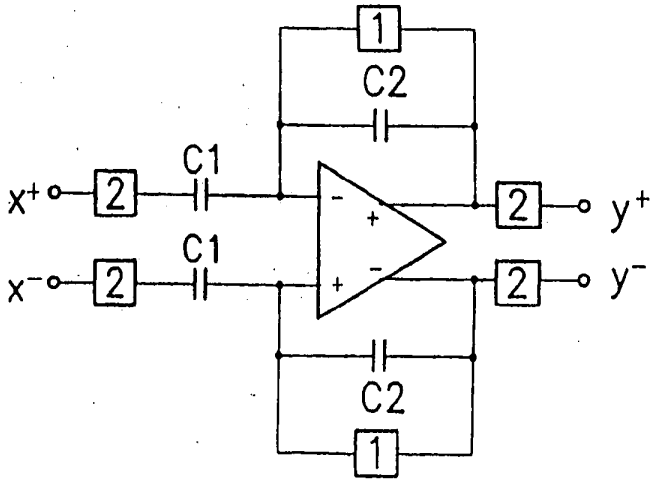


CIRCUIT DIAGRAM

FIG. 6(b)

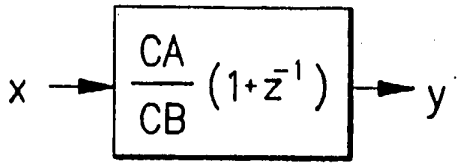


Z-DOMAIN SYMBOL

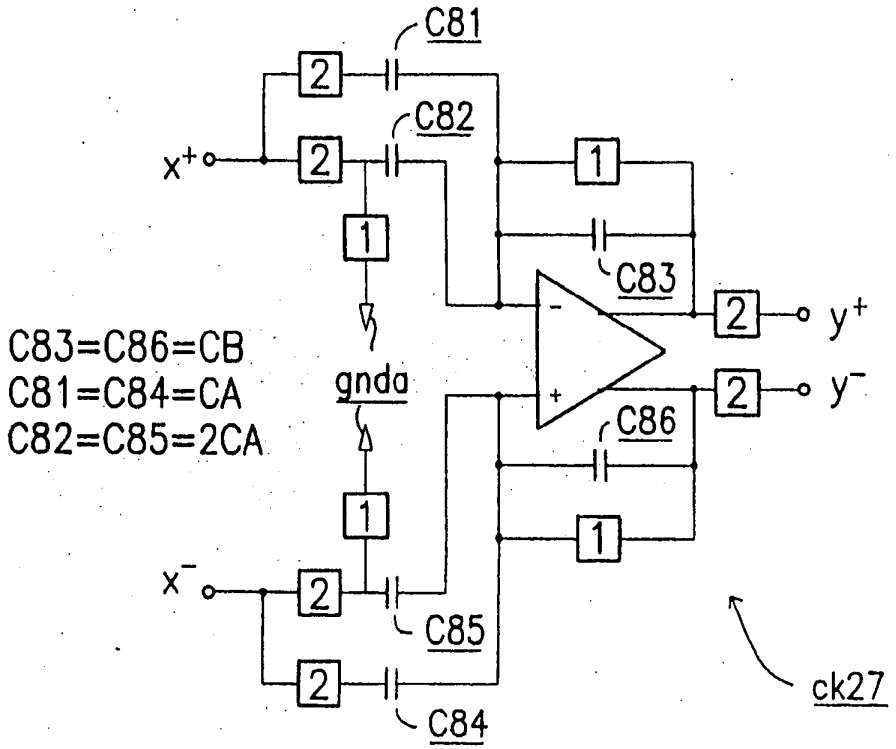


CIRCUIT DIAGRAM

FIG. 7(a)(PRIOR ART)



Z-DOMAIN SYMBOL



CIRCUIT DIAGRAM

FIG. 7(b)

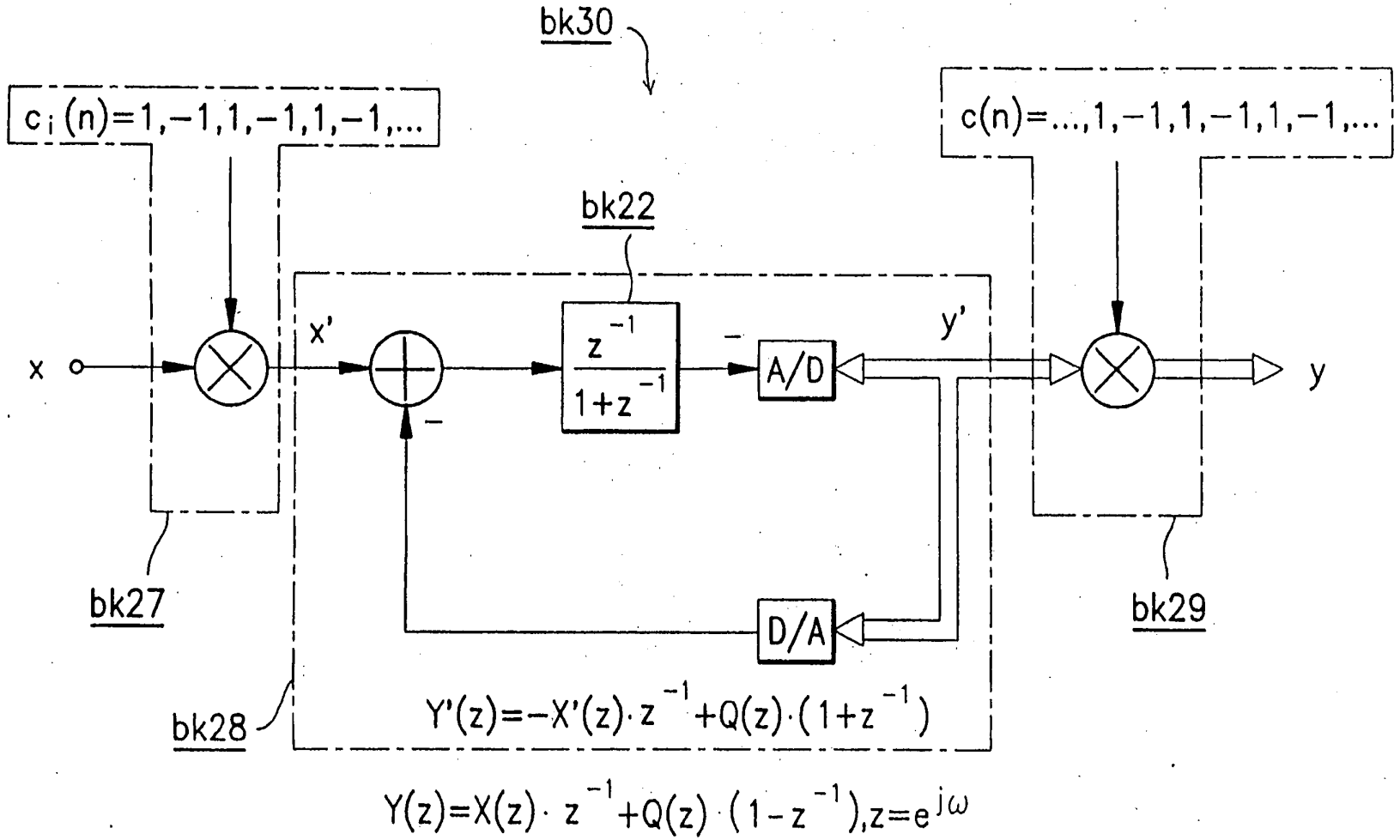

bk30
$c_i(n)=1,-1,1,-1,1,-1,...$
$c(n)=...,1,-1,1,-1,1,-1,...$
bk22
x
x'
$\frac{z^{-1}}{1+z^{-1}}$
A/D
y'
y
bk27
bk29
D/A
bk28
$Y'(z)=-X'(z)\cdot z^{-1}+Q(z)\cdot(1+z^{-1})$
$Y(z)=X(z)\cdot z^{-1}+Q(z)\cdot(1-z^{-1}),z=e^{j\omega}$

FIG. 8

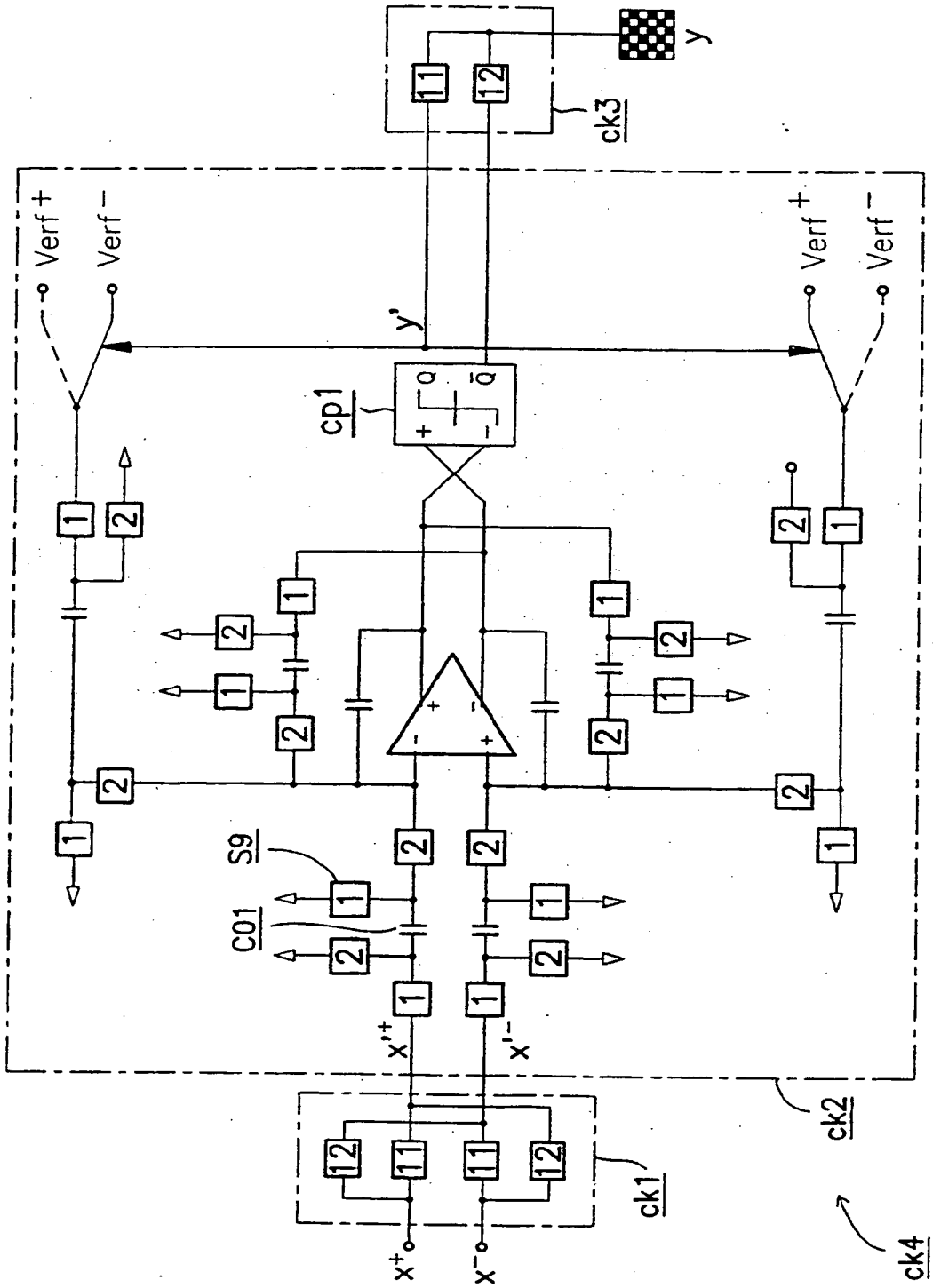


FIG. 9

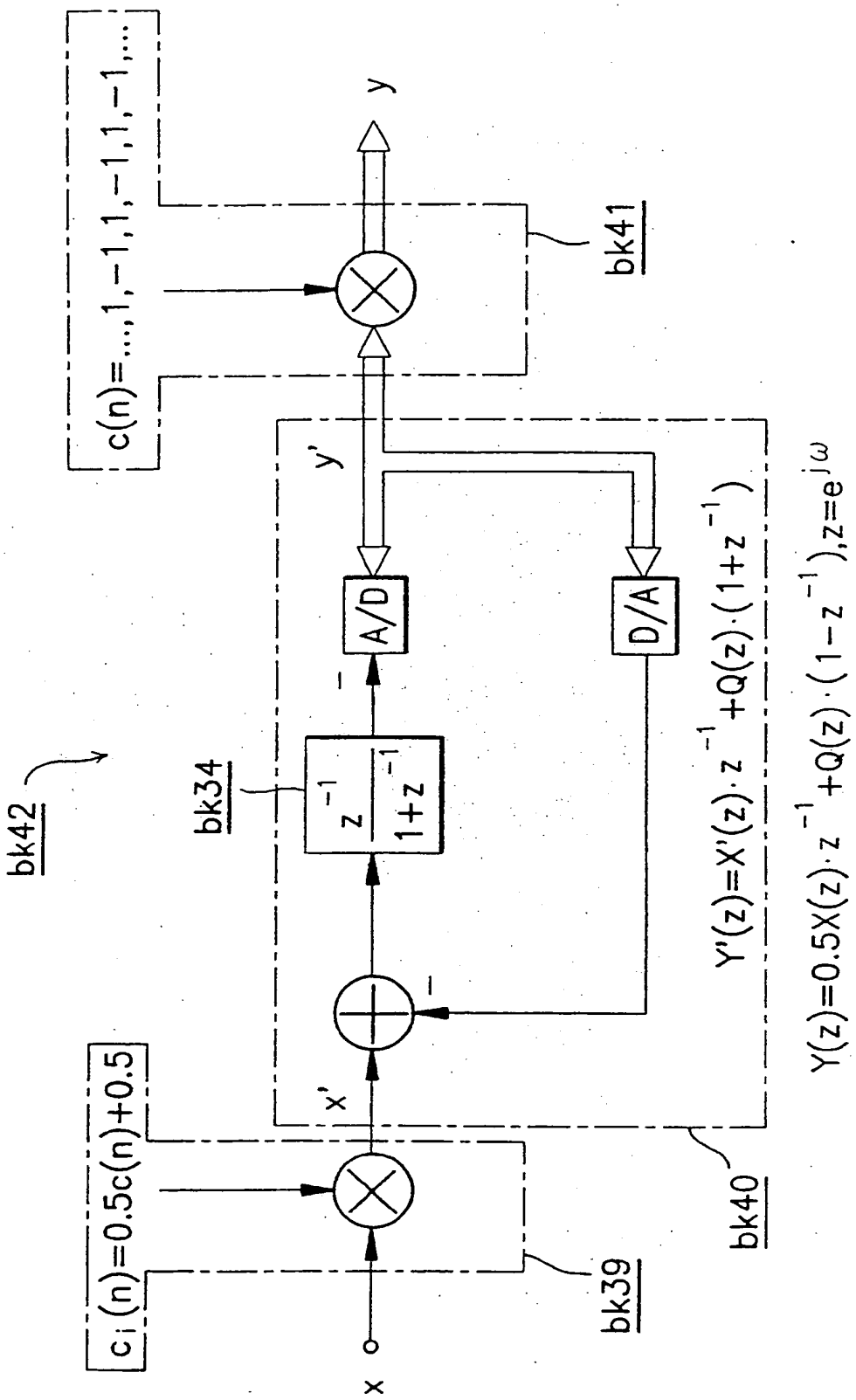


FIG. 10

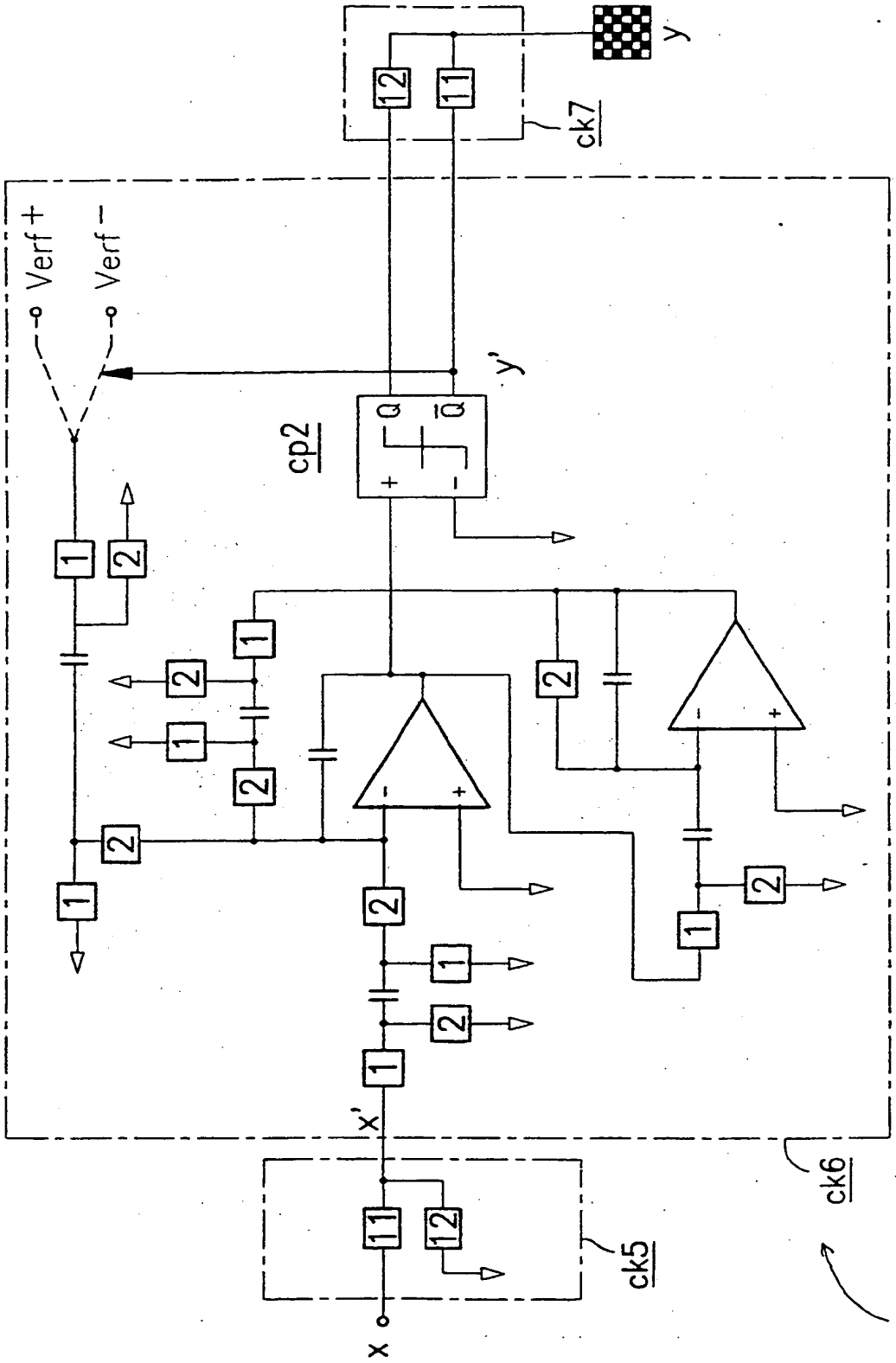


FIG. 11

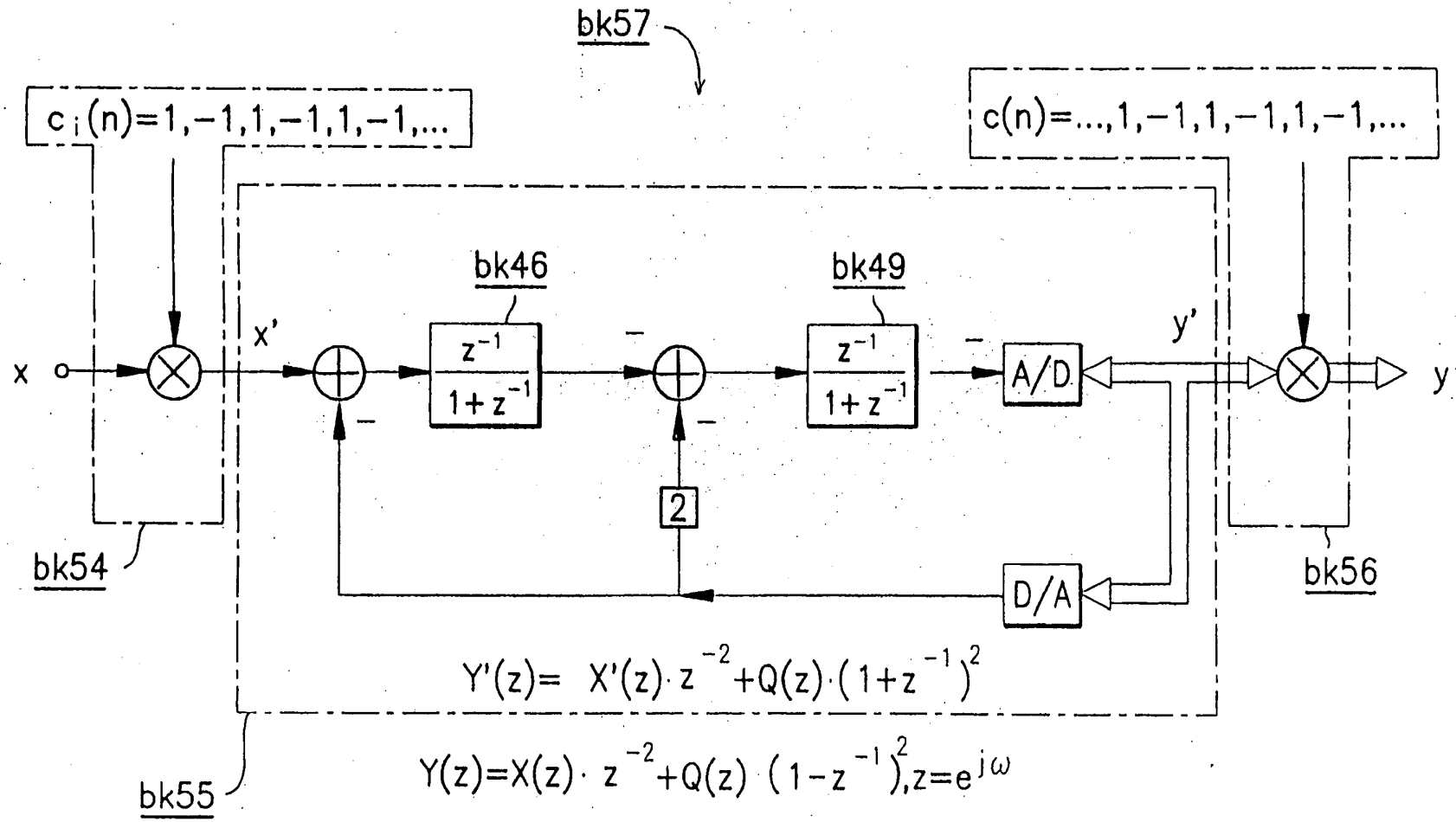

bk57
$c_i(n)=1,-1,1,-1,1,-1,\ldots$
$c(n)=\ldots,1,-1,1,-1,1,-1,\ldots$
bk46
bk49
x
x'
y'
y
$\frac{z^{-1}}{1+z^{-1}}$
$\frac{z^{-1}}{1+z^{-1}}$
A/D
D/A
2
bk54
bk56
bk55
$Y'(z)= X'(z)\cdot z^{-2}+Q(z)\cdot(1+z^{-1})^2$
$Y(z)=X(z)\cdot z^{-2}+Q(z)\ (1-z^{-1})^2, z=e^{j\omega}$

FIG. 12

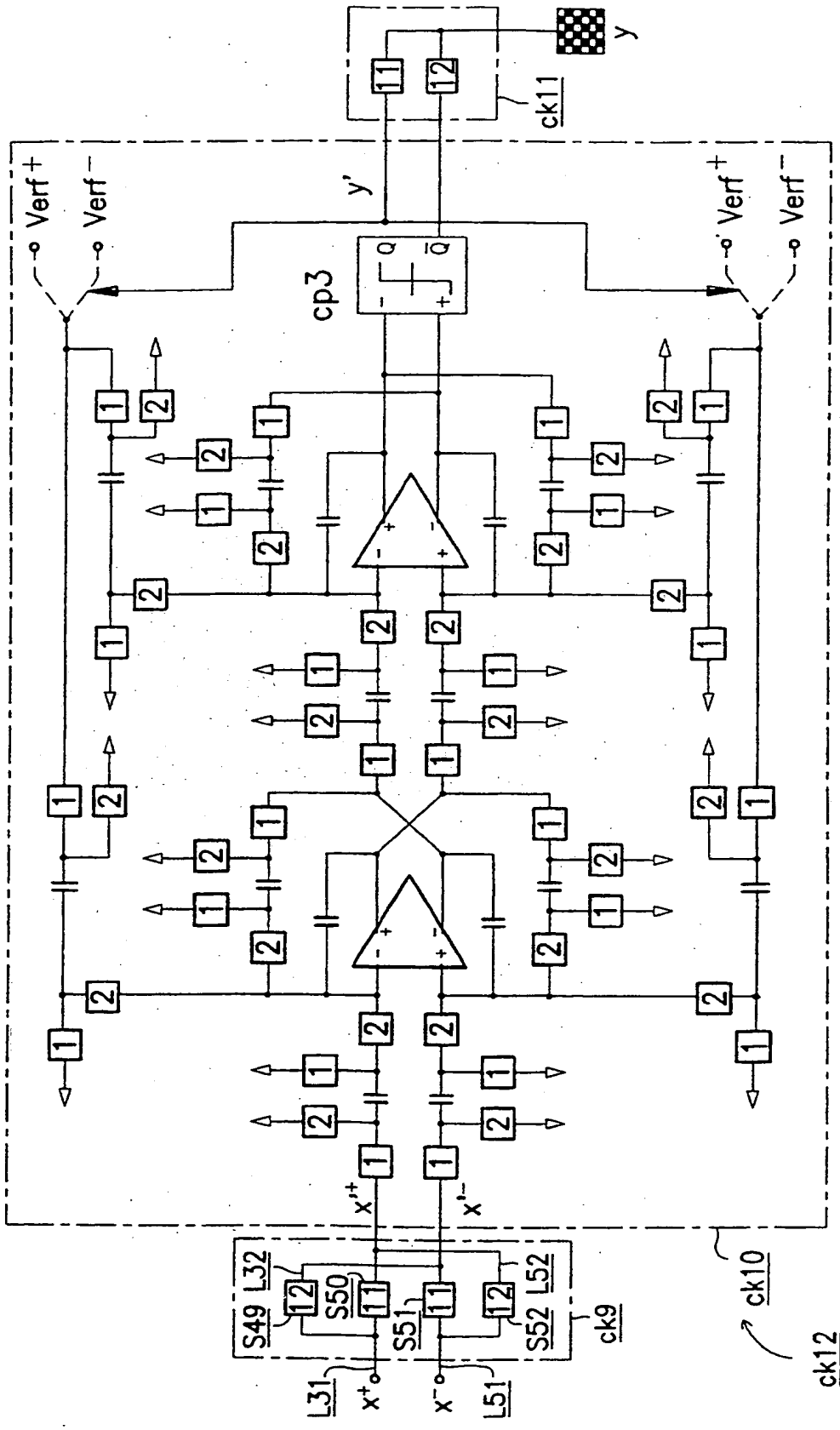
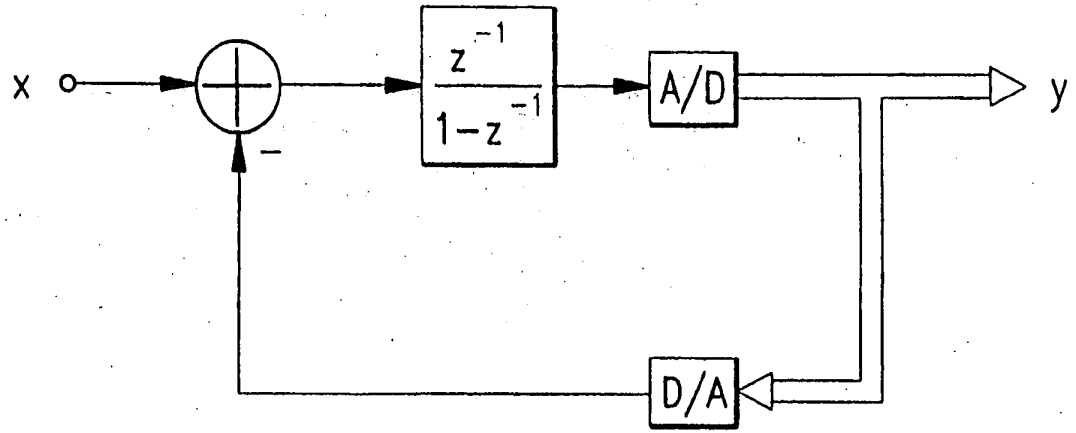

y
ck11
Verf+
Verf−
y'
cp3
Q
Q̄
x''+
x''−
S49 L32
S50
S51
S52 L52
ck9
ck10
ck12
L31
x+
x−
L51

FIG. 13



$$Y(z)=X(z)\cdot z^{-1}+Q(z)\cdot(1-z^{-1}),z=e^{j\omega}$$

FIG. 14(PRIOR ART)

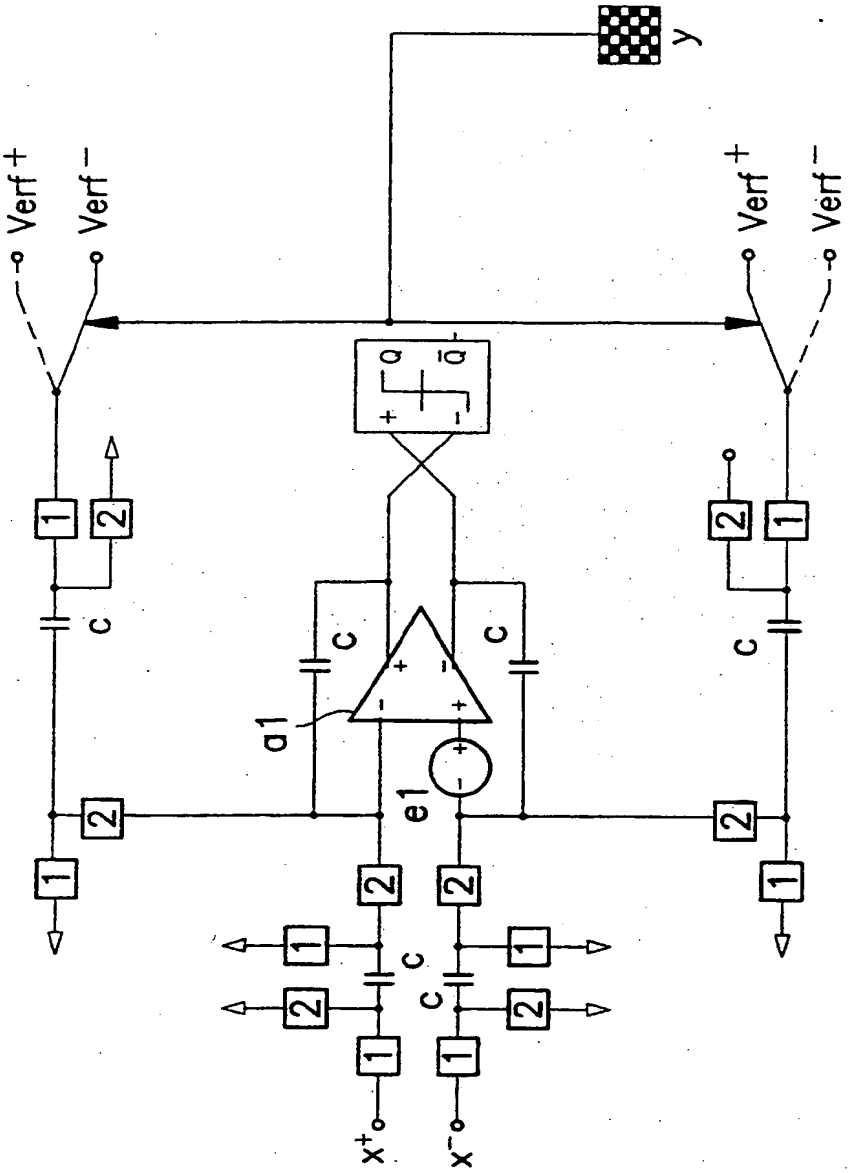
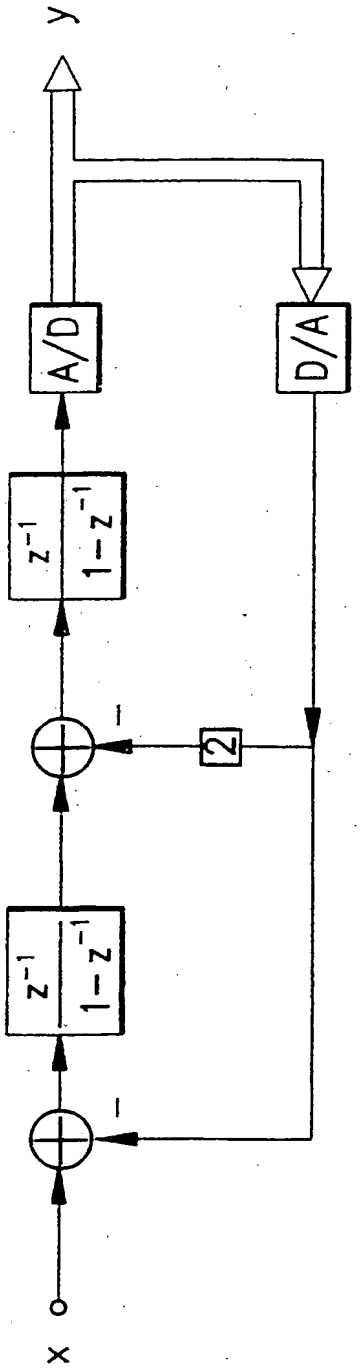


FIG. 15(PRIOR ART)



$$Y(z)=X(z)\cdot z^{-2}+Q(z)\cdot(1-z^{-1})^{2},z=e^{j\omega}$$

FIG. 16(PRIOR ART)

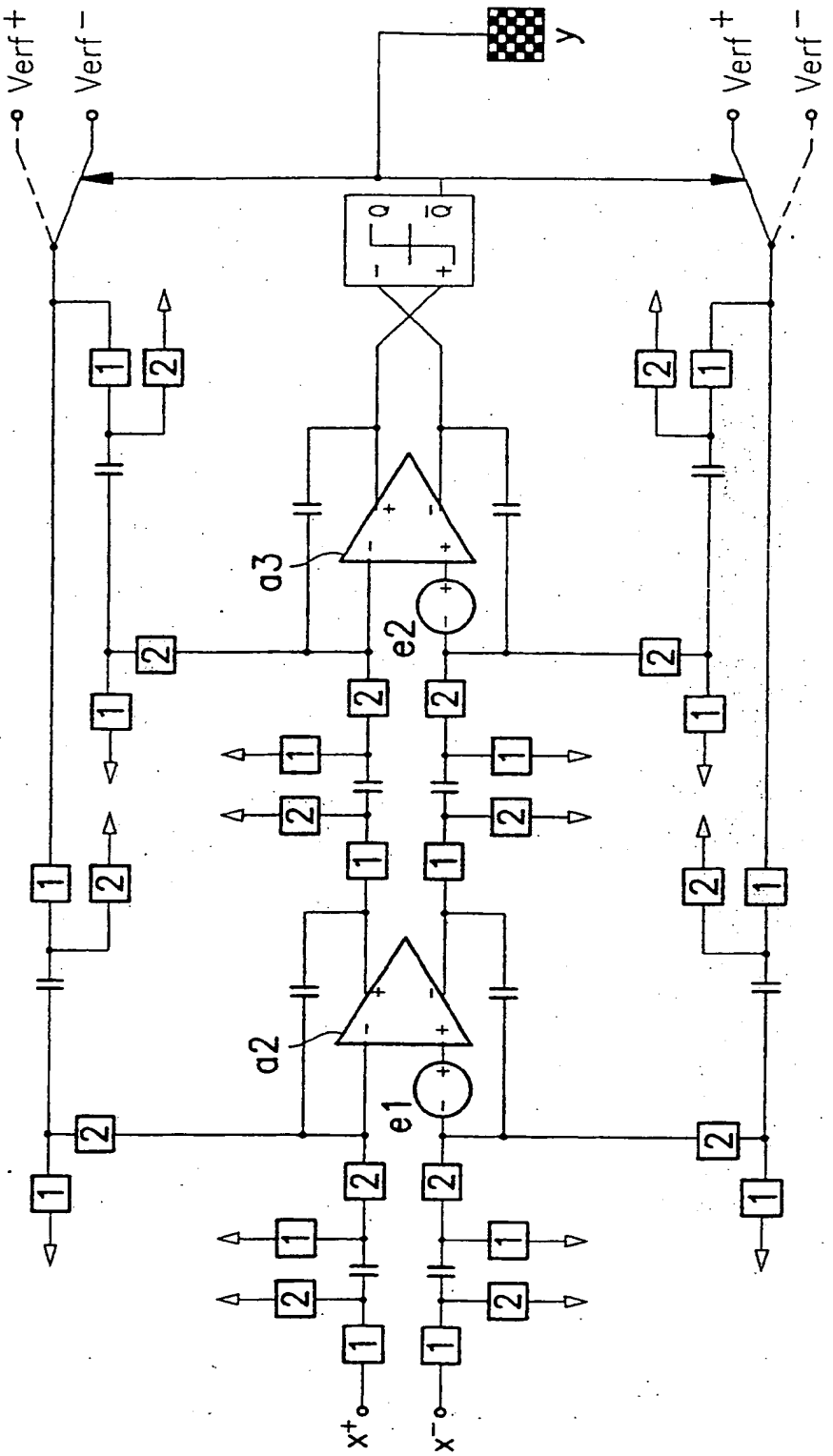


FIG. 17(PRIOR ART)

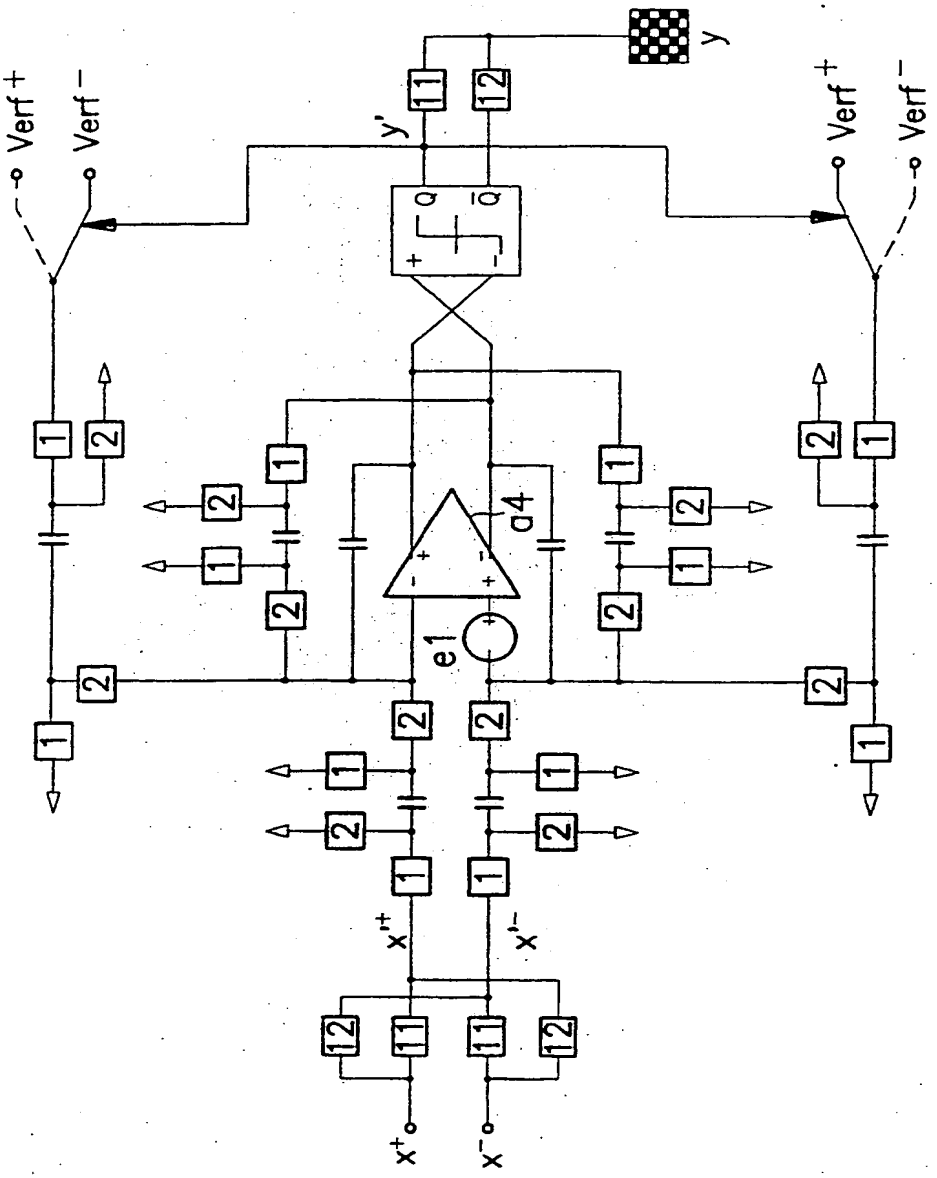


FIG. 18

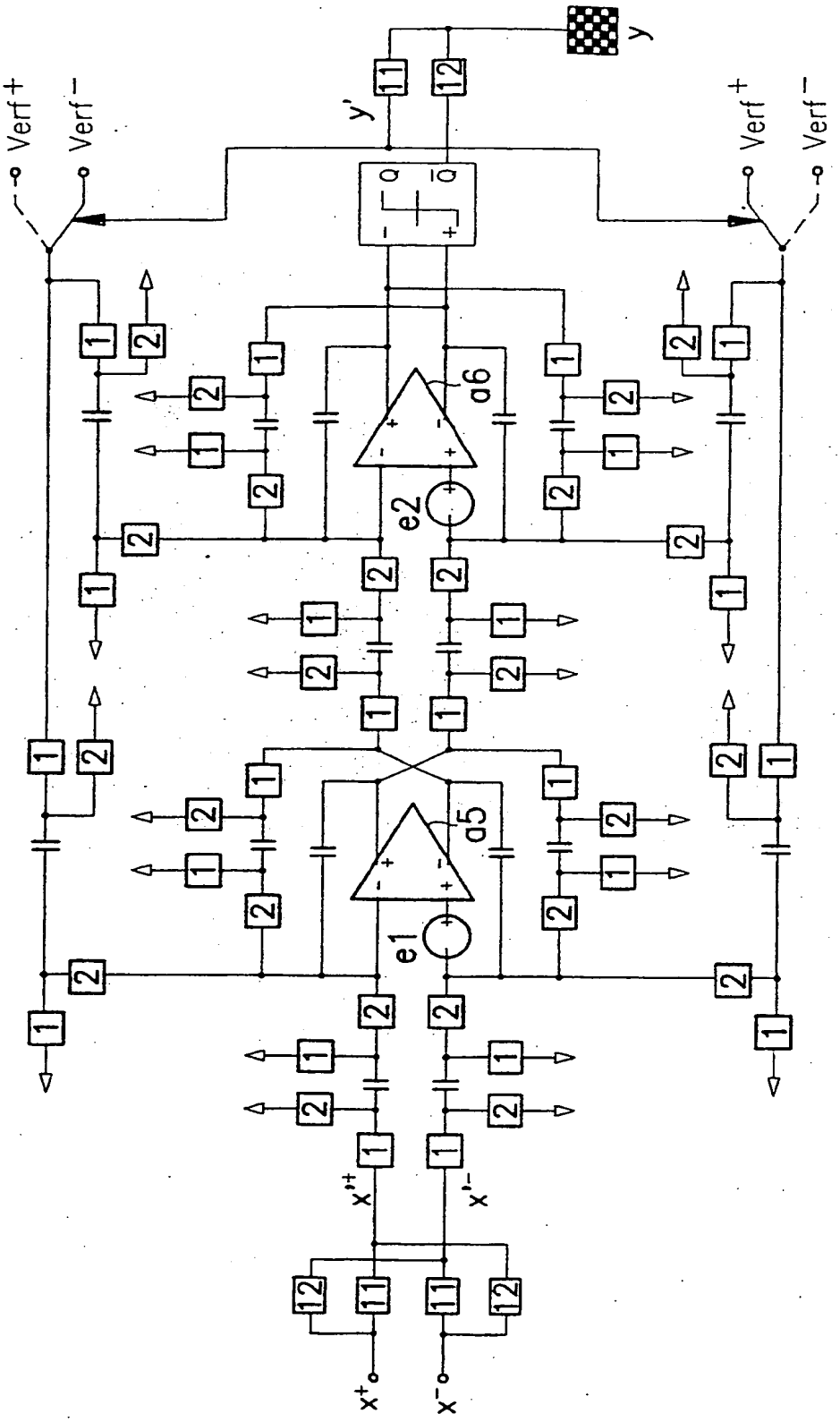


FIG. 19

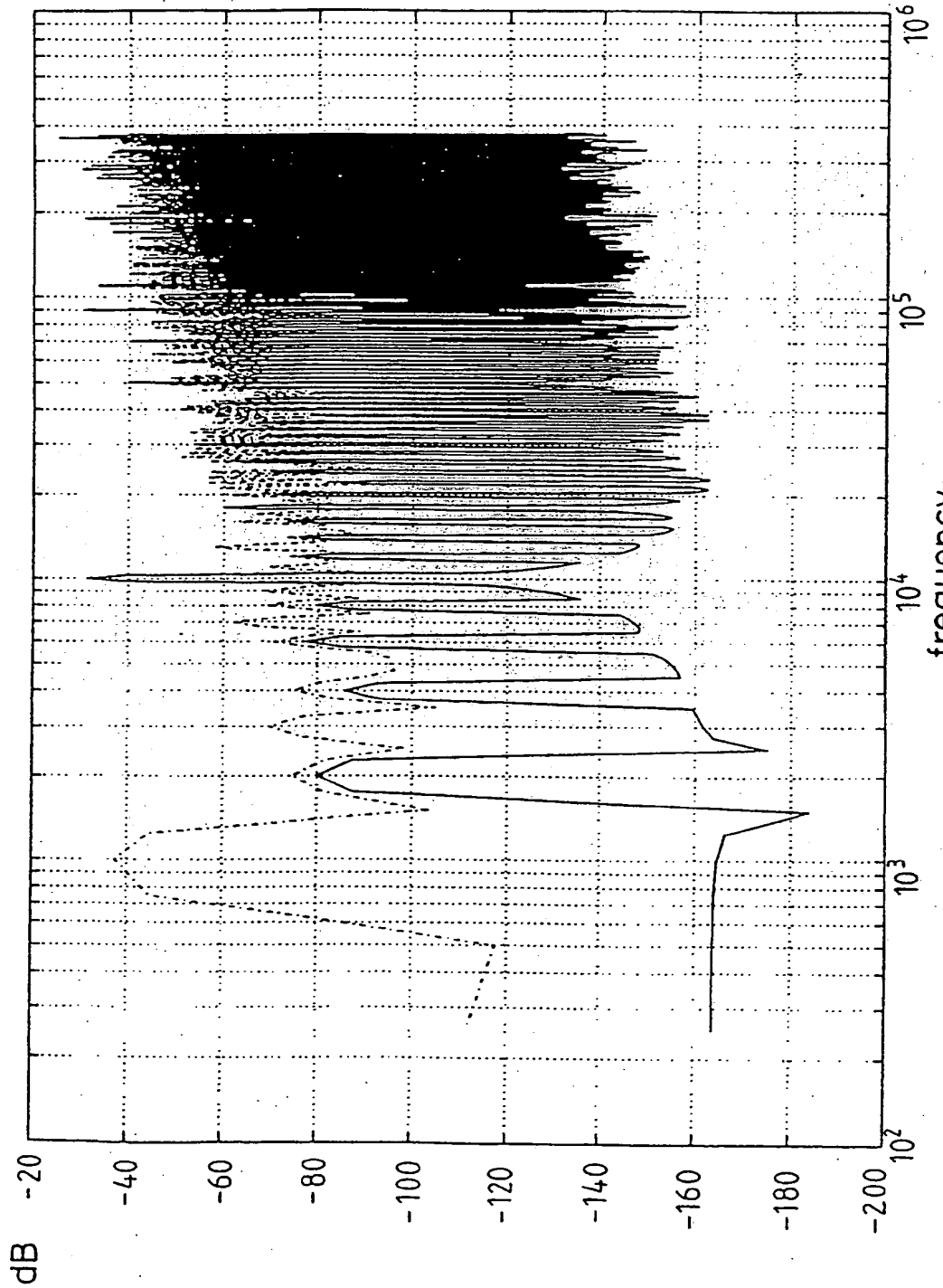


FIG. 20(a)

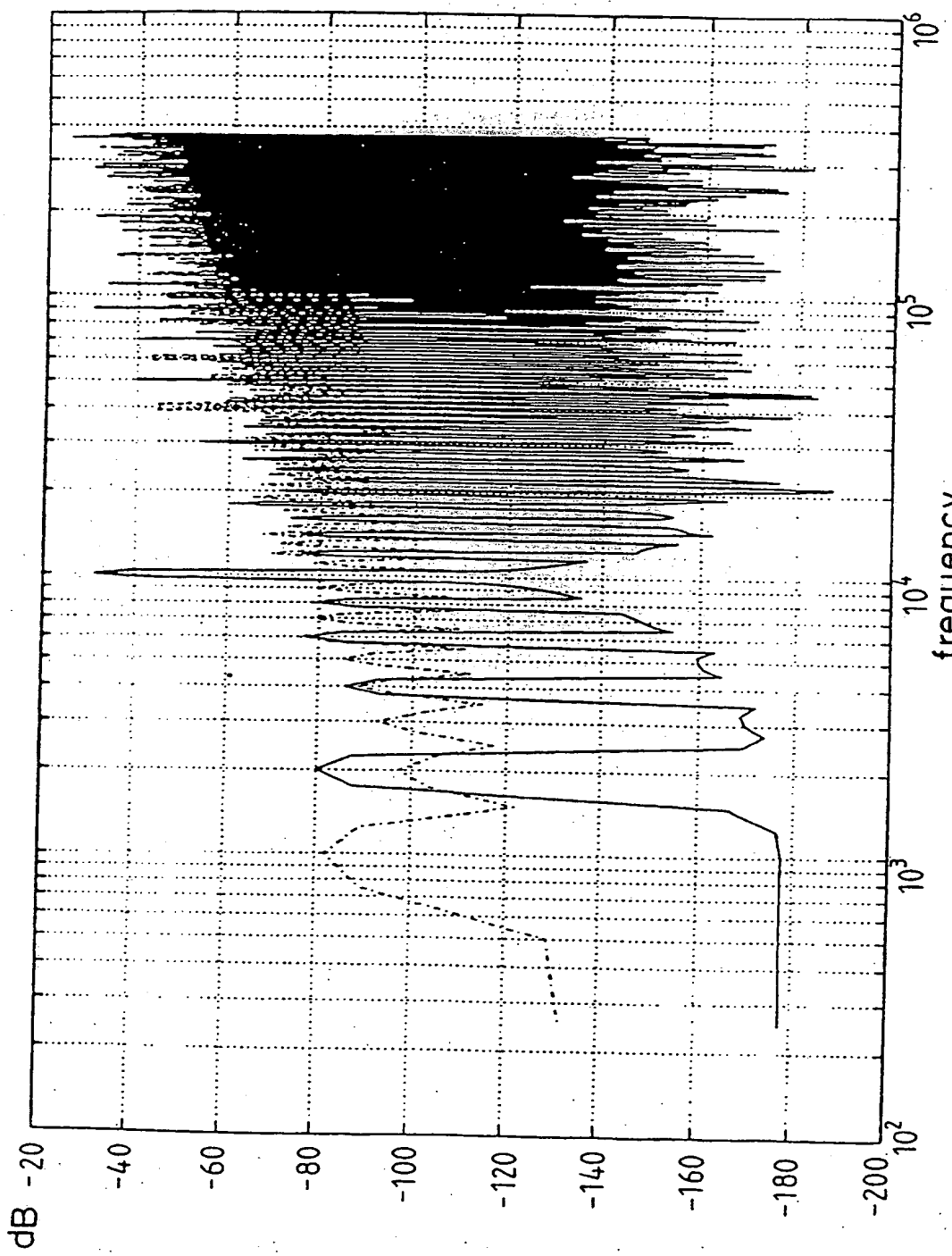


FIG. 20(b)

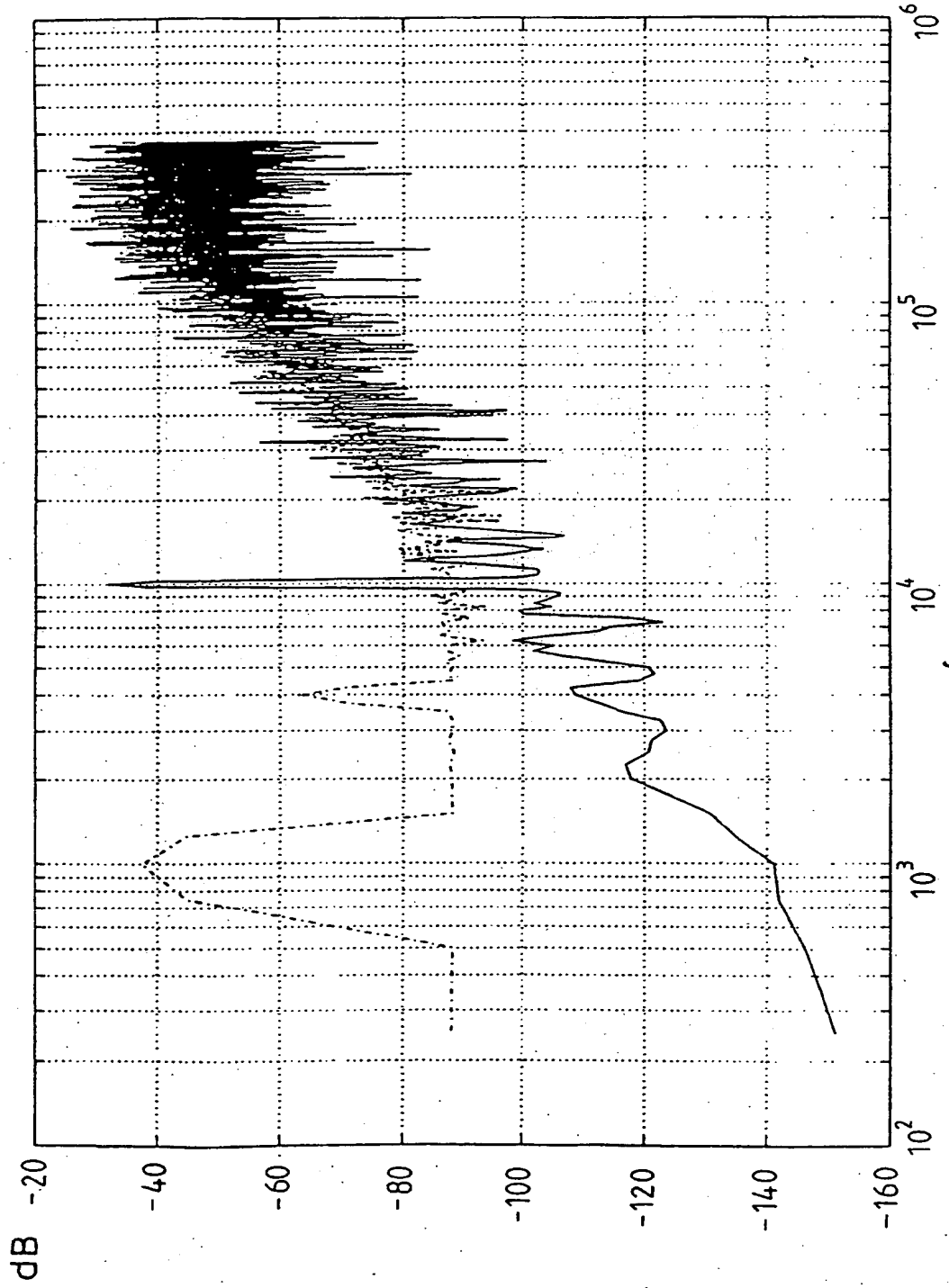


FIG. 21(a)

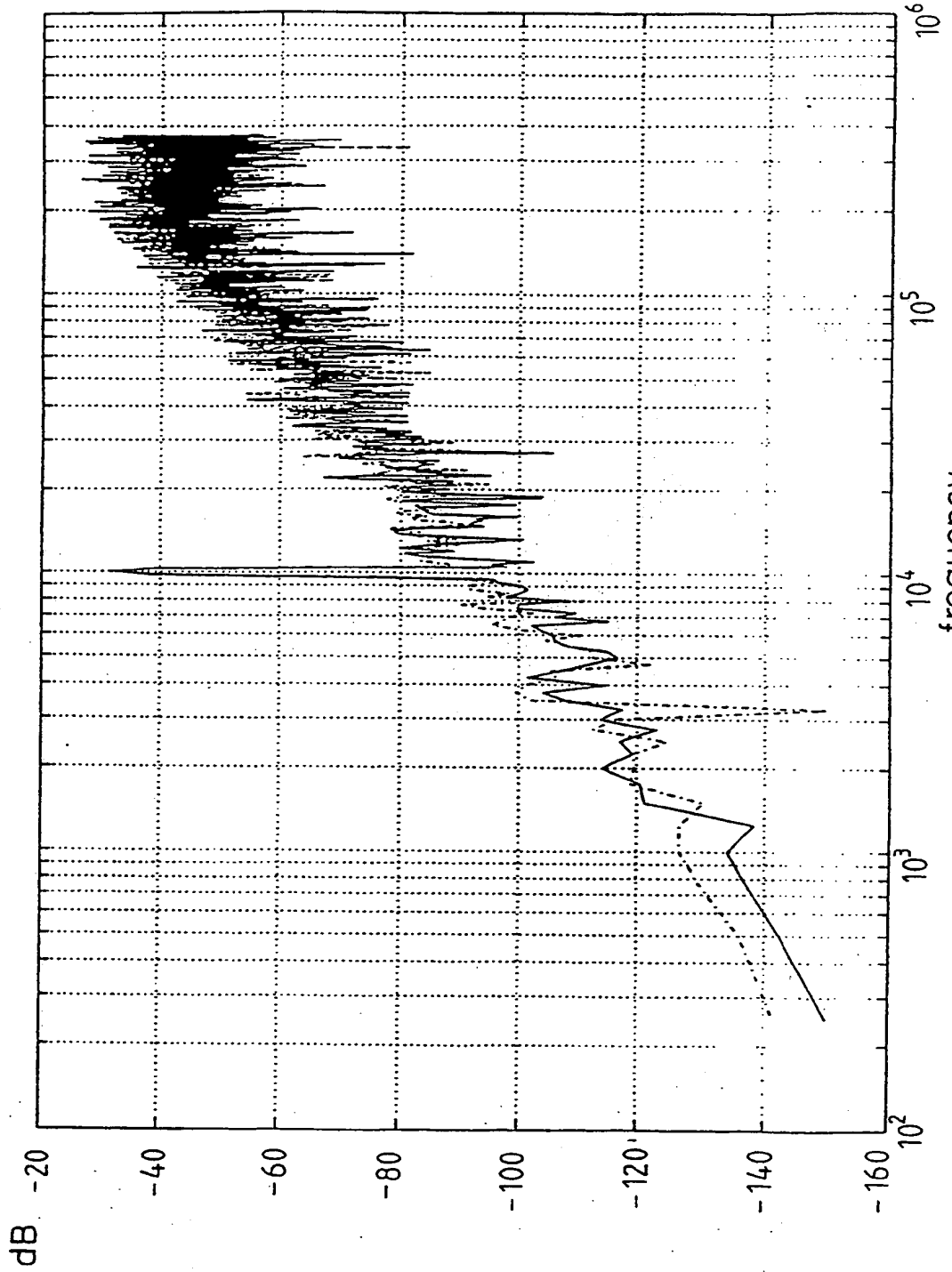


FIG. 21(b)

TITLE

CHOPPER-STABILIZED SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER

BACKGROUND OF THE INVENTION

The present invention relates generally to a analog-to-digital converters(ADC), and more particularly to a chopper-stabilized sigma-delta ADC using a chopper stabilizer to remove the circuit low-frequency noises, so that the resolution of the sigma-delta ADC is greatly increased.

At present, the interface circuits of the sigma-delta ADC have been widely used in the VLSI(Very Large-Scale Integration) application products. For example, in case of the telecommunication products, they can be applied to the integrated service digital network (ISDN) U-interface, 9600 MODEM(Modem V.32 9600 bps), pulse code modulation codedecoder (PCM CODEC), etc. In comsumer electronic products, they can be applied to digital audio tape (DAT) recorders, compact disc (CD) player systems, and so on. In instrumentation products, they can be applied to 5 1/2 digital panel meters which can resolve a 1 μV signal. In these system, only the digital processing (DSP) chip connected behind the sigma-delta ADC needs to be differently designed to meet the requirements for different products. Therefore, it can be seen that the sigma-delta ADC is generally applied to various IC (Integrated Circuit) application products.

Referring to Figs. 14 and 15, conventional sigma-delta ADCs are typically constituted by a switched-capacitor circuit. Such a technology can refer to S. R. Norsworth, "Oversampled Sigma-Delta Data Converter", *ISCAS'90* Workshop, New Orleans, LA, April 30, 1990. The sigma-delta ADC is a discrete-time system, and its relationship between input and output signals can be described in z-domain wherein $z=e^{jw}$, and w is an angular frequency. The relationship between w and the continuous signal frequency f can be characterized by $w=2\pi f/f_S$, wherein f_S is the sampling frequency of system. The sampling frequency fs= 1/T, wherein T is the sampling period. If the continuous signal frequency $f= f_S/2$, the angular frequency $w = \pi$. In this specification, the description for the sigma-delta ADC are all in z-domain.

Referring to Figs. 1(a) to 1(e), there is shown a conventional sigma-delta ADC 10, and its transfer function can be characterized in z-domain by

$$Y(z)=X(z)ST(z)+ Q(z)NT(z),\ z=e^{jw}$$

wherein ST(z) is signal transfer function, and NT(z) is a noise transfer function. As shown in Fig. 1(b), the signal transfer function ST(z) is characterized by having a passband in the low-frequency range to permit the input low-frequency signal passing through. As shown in Fig. 1(c), the noise transfer function NT(z) is characterized by having a very high attenuation in the low-frequency range to attenuate a large part of the low-frequency quantization noise which is generated when the input signal passes

through the analog-to-digital converter A/D (this A/D is a low-bit analog-to-digital converter, and usually outputs only one bit) of the sigma-delta ADC 10. In this way, the quantization noise will not be too large in the low-frequency portion to interfere the passing of the normal signal. As shown in Figs. 1(d) and 1(e), the quantization noise generated when the input signal x passes through the sigma-delta ADC 10 is very small in low-frequency portion. However, since the signal transfer function ST(z) has a passband in the low-frequency range, the other circuit low-frequency noises (except the quantization noise), for example the 1/f noise and the offset voltage of the operational amplifier, will also pass through the sigma-delta ADC 10 at the same time as the normal low-frequency signal, so that the output digital signal y will be contaminated. Therefore, circuit low-frequency will limit the sigma-delta ADC 10 to reach higher resolution, for example $\geq$ 16 bits.

Known methods of reducing the low-frequency in a sigma-delta ADC circuit are usually derived from method of reducing the low-frequency noise in conventional switched-capacitor circuits, for example use of a chopper-stabilized operational amplifier to replace the operational amplifier(may refer to U.S. Patent No. 4,939,516) or the correlated double sampling technology. Since these methods all solve this low-frequency noise problem from the circuit angle, they can only overcome part of the problem.

Typical examples of the prior sigma-delta ADC are shown in Figs. 14 to 17. Fig. 14 shows a prior 1-order sigma-delta ADC structure, and Fig. 15 shows a circuit designed on the basis of the structure shown in Fig. 14. Fig. 16 shows a prior single-input-to-single-output 2-order one-bit sigma-delta ADC structure, and Fig. 17 shows a circuit designed on the basis of the structure shown in Fig. 16. the blocks of $Z^{-1}/(1-Z^{-1})$ can be e implemented by the circuit as shown in Fig. 5(b). Since the structures and circuits shown in Figs. 5(b), 14, to 17 are all clear to those skilled in the art, it is deemed unnecessary to describe them further. Other prior sigma-delta ADCs are constituted by similar manner, as shown in U.S. Patent Nos. 5,068,660; 4,983,975; 4,972,436; 4,972,360; 4,939,516; and 4,920,544.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a chopper-stabilized sigma-delta analog-to-digital converter(ADC) to solve the above-mentioned low-frequency noise problem and thus to greatly increase the resolution of the sigma-delta ADC. The present invention approaches this problem from the system angle and technology, quite different from the circuit angle in the prior arts.

Another object of the present invention is to provide a chopper-stabilized sigma-delta ADC which has a simple circuit complexity , is easy to design and can be manufactured without any special processing technologies.

In accordance with the present invention, a chopper-stabilized sigma-delta analog-to-digital converter comprises:

a first discrete-time multiplier adapted to receive an analog input signal and a first discrete-time sequence, and capable of multiplying the analog input signal by the first discrete-time sequence to produce a choppered analog signal; and

a chopper sigma-delta analog-to digital converter (ADC) connected in series to the first discrete-time multiplier in order to receive an convert the choppered analog signal into a digital output signal, the chopper sigma-delta ADC being characterized in z-domain by:

$$Y'(z)=X'(z)ST'(z)+ Q(z)NT'(z),\ z=e^{jw}$$

wherein ST'(z) is a signal transfer function, and is characterized by having a passband in a high-frequency range; and NT'(z) is a noise transfer function, and characterized by having a high attenuation in the high-frequency range.

In accordance with another aspect of the present invention, a chopper-stabilized sigma-delta ADC further comprises a second discrete-time multiplier connected in series to the chopper sigma-delta ADC in order to receive the digital output signal, the second discrete-time multiplier adapted to receive a second discrete-time sequence, and multiplying the digital output signal by the

second discrete-time sequence to produce a choppered digital signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reference to the following description and accompanying drawings, which form an integral part of this application:

Figs. 1(a) to 1(e) illustrate the structure and characteristics of a conventional sigma-delta analog-to-digital converter (ADC);

Figs 2(a) to 2(h) illustrate the structure and characteristics of a chopper-stabilized sigma-delta ADC according to a first preferred embodiment of the present invention, which is suitable for a fully-differential circuit implementation;

Figs. 3(a) to 3(h) illustrate the structure and characteristics of a chopper-stabilized sigma-delta ADC according to a second preferred embodiment of the present invention, which is suitable for a single-input-to-to single-output circuit implementation;

Figs. 4 shows the control clocks indicated in all circuit diagrams of the drawings;

Figs. 5(a) and 5(b) illustrate the z-domain symbols and circuit diagrams of two conventional single-input-to-single-output building blocks;

Fig. 5(c) illustrate the z-domain symbol and circuit diagram of a single-input-to-single-output building block according to the present invention;

Fig. 6(a) illustrate the z-domain symbol and circuit diagram of a conventional fully-differential building block;

Fig. 6(b) illustrate the z-domain symbol and circuit diagram of a fully-differential building block according to the present invention;

Fig. 7(a) illustrate the z-domain symbol and circuit diagram of a conventional gain building block;

Fig. 7(b) illustrate the z-domain symbol and circuit diagram of a gain building block according to the present invention;

Fig. 8 is a structural block diagram of a 1-order chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure as shown in Fig. 2;

Fig. 9 is a schematically electrical diagram of a fully-differential 1-order one-bit chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure of Fig. 8;

Fig. 10 is a structural block diagram of a 1-order chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure as shown in Fig. 3;

Fig. 11 is a schematically electrical diagram of a single-input-to-single-output 1-order one-bit chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure of Fig. 10;

Fig. 12 is a structural block diagram of a 2-order chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure as shown in Fig. 2;

Fig. 13 is a schematically electrical diagram of a fully-differential 2-order one-bit chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure of Fig. 12;

Fig. 14 is a structural block diagram of a conventional 1-order sigma-delta ADC;

Fig. 15 is a schematically electrical diagram of a conventional 1-order sigma-delta ADC circuit designed on the basis of the structure of Fig. 14, wherein an equivalent noise source is added;

Fig. 16 is a structural block diagram of a conventional 2-order sigma-delta ADC;

Fig. 17 is a schematically electrical diagram of a conventional 2-order sigma-delta ADC circuit designed on the basis of the structure of Fig. 16, wherein two equivalent noise sources are added;

Fig. 18 is similar to Fig. 9, but an equivalent noise source is added further;

Fig. 19 is similar to Fig. 13, but two equivalent noise source are added further;

Figs. 20(a) and 20(b) show the simulation spectrums of the circuits as shown in Figs. 15 and 18; and

Figs. 21(a) and 21(b) show the simulation spectrums of the circuits as shown in Figs. 17 and 19.

Figs. 21(a) and 21(b) show the simulation spectrums of the circuits as shown in Figs. 17 and 19.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In this description, two kinds of chopper-stabilized sigma-delta analog-to-digital converters (ADCs) of the present invention are disclosed. Fig. 2(a) shows the first kind of chopper-stabilized sigma-delta ADC structure bk9 which is suitable for a fully-differential circuit implementation. Fig. 3(a) shows the second kind of chopper-stabilized sigma-delta ADC structure bk18 which is suitable for a single-input-to-single-output circuit implementation.

Referring now to Fig. 2(a), the chopper-stabilized sigma-delta ADC structure bk9 according to the first preferred embodiment of the present invention includes a discrete-time multiplier bk1, a chopper sigma-delta ADC bk3, and another discrete-time multiplier bk4, connected together in series. The discrete-time multiplier bk1 receives an input analog low-frequency signal x, and a discrete-time sequence bk2 consisting of alternating "1" and "-1" digital signals, and multiplies them to produce a signal x'. The chopper sigma-delta ADC bk3 especially designed by the present invention receives and converts the output signal x' of the discrete-time multiplier bk1 into a digital signal output y'. The discrete-time multiplier bk4 receives the output signal y' of the chopper sigma-delta ADC bk3, and a discrete-time sequence bk5 consisted of alternating "1" and "-1" digital signals, and multiplies them to produce a

digital output signal y for the entire chopper-stabilized sigma-delta ADC bk9.

Referring to Figs. 2(a) to 2(h), Figs. 2(b) to 2(d) illustrate the characteristics of the chopper sigma-delta ADC bk3, and Figs. 2(e) to 2(h) are diagrams of the half-spectrums of respective signals at different points in the chopper-stabilized sigma-delta ADC bk9. The multiplication operation conducted by the discrete-time multiplier bk1 is called a "chopper" multiplication, and can modulate the input low-frequency signal x having a center frequency at w_x, as shown in Fig. 2(e), into a signal having a center frequency at $(\pi + w_x)$ which, in the half-spectrum, is represented by a signal x' having a center frequency at $(\pi - w_x)$, as shown in Fig. 2(f). The transfer function of the chopper sigma-delta ADC bk3 can be characterized in the z domzin by:

$$Y'(z)=X'(z)ST'(z) + Q(z)NT'(z),\ z=e^{jw}$$

wherein ST'(z) is the signal transfer function, and NT'(z) is the noise transfer function. As shown in Fig. 2(c), the signal transfer function ST'(z) is characterized by having a passband in the high-frequency range, i.e. the area around the angular frequency π, to permit the input high-frequency signal, i.e. the signal around the angular frequency π, to pass through. As shown in Fig. 2(d), the noise transfer function NT'(z) is characterized by having a very high attenuation in the high-frequency range to attenuate a large part of the quantization noise in high-frequency which is

generated when the input signal passes through the analog-to-digital converter A/D(this A/D is a low-bit analog-to-digital converter, and usually outputs only one bit) of the chopper sigma-delta ADC bk3. In this way, the quantization noise will not be too large in high-frequency portions to interfere with the passing of the normal high-frequency signal. Fig. 2(g) shows the spectrum of the output digital signal y', and the circuit low-frequency noise joins in at this time. The "chopper" multiplication of the discrete-time multiplier bk4 choppers the output signal y' of the chopper sigma-delta ADC bk3 to produce the finally desired digital signal y. The spectrum of the digital signal y is shown in Fig. 2(h). In this way, there is only a small quantization noise in the low-frequency range, and the circuit low-frequency noise is choppered to the high-frequency range by the "chopper" multiplication of the discrete-time multiplier bk4, so as not to affect the resolution. Since both of the input and output signals of the discrete-time multiplier bk4 are all in digital forms, the discrete-time multiplier bk4 may be designed in the digital signal processing(DSP) chip connected behind the sigma-delta ADC. That is to say, the chopper-stabilized sigma-delta ADC bk9 of the present invention may omit the discrete-time multiplier bk4.

Referring now to Fig. 3(a), the chopper-stabilized sigma-delta ADC structure bk18 according to the second preferred embodiment of the present invention includes a

discrete-time multiplier bk10, a chopper sigma-delta ADc bk12, and another discrete-time multiplier bk13, connected together in series. The discrete-time multiplier bk10 receives an input analog low-frequency signal x, and a discrete-time sequence bk11 consisting of alternating "1" and "0", and multiplies them to produce a signal x'. The chopper sigma-delta ADC bk12 also especially designed by the present invention receives and converts the output signal x' of the discrete-time multiplier bk10 into a digital signal output y'. The discrete-time multiplier bk13 receives the output signal y' of the chopper sigma-delta ADC bk12, and a discrete-time sequence bk14 consisting of alternating "1" "-1", and multiplies them to produce a digital output signal y for the entire chopper-stabilized sigma-delta ADC bk18.

Referring to Figs. 3(a) to 3(h), Figs. 3(b) to 3(d) illustrate the characteristics of the chopper sigma-delta ADC bk12, and Figs. 3(e) to 3(h) are schematic diagrams of the half-spectrums of respective signals at different points in the chopper-stabilized sigma-delta ADc bk18. The "chopper" multiplication conducted by the discrete-time multiplier bk10 which receives the discrete-time sequence bk11 obtains a little different result from the "chopper" multiplication conducted by the discrete-time multiplier bk1 which receives the discrete-time sequence bk2 as shown in Fig. 2(a). The discrete-time multiplier bk10 modulates only half of the input low-frequency signal x having a center frequency at w_x, as shown Fig. 3(e), into a signal having a

center frequency at ($\pi + w_x$) which, in the half-spectrum, is represented by a signal having a center frequency at ($\pi - w_x$), while the other half of the input signal x still stays in the low-frequency range, as shown in Fig. 3(f). The transfer function of the chopper sigma-delta ADC bk12 can be characterized in the z domzin:

$$Y'(z)=X'(z)ST'(z)+ Q(z)NT'(z),\ z=e^{jw}$$

wherein ST'(z) is the signal transfer function, and NT'(z) is the noise transfer function. As shown in Fig. 3(c), the signal transfer function ST'(z) is characterized by having a passband in the high-frequency range to permit the input high-frequency signal passing through. As shown in Fig. 3(d), the noise transfer function NT'(z) is characterized by having a very high attenuation in the high-frequency range to attenuate a large part of the quantization noise in high-frequency which is generated when the input signal passes through the analog-to-digital converter A/D (this A/D is a low-bit analog-to-digital converter, and usually outputs only one bit) of the chopper sigma-delta ADC bk12. In this way, the quantization noise will not be too large in high-frequency portion to interfere the passing of the normal high-frequency signal. Fig. 3(g) shows the spectrum of the output digital signal y', and the circuit low-frequency noise joins in at this time. The "chopper" multiplication of the discrete-time multiplier bk13 choppers the output signal y' of the chopper sigma-delta ADC bk12 to produce the final output digital signal y. The spectrum of the digital

signal y is shown in Fig. 3(h). In this way, the circuit low-frequency noise is choppered to the high-frequency range by the "chopper" multiplication of the discrete-time multiplier bk13, so as not to affect the resolution. In addition, there will be a 0.5-time linear error in this embodiment because only half of the input low-frequency signal x is modulated to the high-frequency range, i.e. the input low-frequency signal x is half attenuated before entering the analog-to-digital converting process. However, this linear error can be compensated in the digital signal processing chip later. Since both of the input and output signals of the discrete-time multiplier bk13 are all in digital form, the discrete-time multiplier bk13 may be designed in the digital signal processing (DSP) chip connected behind the sigma-delta ADC. That is to say, the chopper-stabilized sigma-delta ADC bk18 of the present invention my omit the discrete-time multiplier bk13.

In sum, the function of the chopper-stabilized sigma-delta ADC structure bk9 in accordance with the first embodiment of the present invention can be characterized in z-domain by:

$$Y(z)=X(z)ST(z) + Q(z)NT(z),\ z=e^{jw}$$

That is to say, it achieves the same transfer function as the conventional sigma-delta ADC. The function of the chopper-stabilized sigma-delta ADC structure bk18 in accordance with the second embodiment of the present invention can be characterized in z-domain by:

$$Y(z)=0.5X(z)\ ST(z) + Q(z)NT(z),\ z=e^{jw}$$

It also achieves the same transfer function as the conventional sigma-delta ADC, except a 0.5-time linear error. As mentioned above, this linear error can be compensated in the DSP chip. Therefore, the chopper-stabilized sigma-delta ADC structures bk9 and bk18 not only can achieve the same function as the conventional sigma-delta ADC, but also can remove the circuit low-frequency noises so as to increase the resolution of the converter.

The two above-described structures of the present invention can be implemented by the switched-capacitor circuit. Three application circuit examples are described hereinafter for reference. It should be noted that the control signals of all circuits in the drawings are shown in Fig. 4, and include six control clocks 1, 2, 11, 12, 21, 22. The period T shown in Fig. 4 corresponds to the system sampling frequency of the structures of the present invention. Referring to Fig. 4, the clocks 1 and 2 have the same sampling period T, and are not overlapped with each other. The clocks 11 and 12 have the same sampling period 2T, and are not overlapped with each other while overlapped with the clock 1. The clock 21 and 22 have the same sampling period 2T, and are not overlapped with each other while overlapped with the clock 2. It should be also noted that all blocks A/D in the three examples can be implemented by a comparator, and all blocks D/A can be implemented by a positive/negative voltage output controlled by a one-bit

digital signal. The circuit examples of the other building blocks are shown in Figs. 5(a) to 5(c), 6(a), 6(b), 7(a), and 7(b). In these figures, there are shown the conventional circuit examples, the circuit examples designed for the present invention, and the z-domain symbols of all building block circuits. For example, Fig. 7(a) shows a conventional switched-capacitor differentiator, Figs. 5(c) and 6(b) show two switched-capacitor chopper integrators ck25 and ck26 of the present invention, and Fig. 7(b) shows a switched-capacitor chopper differentiator ck27. Since these circuits are clear to those skilled in the are, it is deemed unnecessary to be described further.

With reference to Fig. 8, there is shown a 1-order chopper-stabilized sigma-delta ADC structure bk30 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the chopper-stabilized sigma-delta ADC structure bk9 of the present invention as shown in Fig. 2(a). Fig. 9 shows a fully-differential 1-order one-bit chopper-stabilized sigma-delta ADC circuit ck4 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure bk30 of Fig. 8. The blocks bk27, bk28, and bk29 in the structure bk30 of Fig. 8 correspond to the circuit blocks ck1, ck2, and ck3 in the circuit ck4 of Fig. 9, respectively. The building block bk22 in the structure bk30 of Fig. 8 may be implemented by the circuit ck26 shown in Fig. 6(b). The block bk27 may be implemented by using the clocks 11 and 12 to control the differential signals, as shown in Fig. 9. The block bk29

may be implemented by using the clocks 11 and 12 to control the positive logic (Q) and negative logic (Q) of the comparator cp1, as shown in Fig. 9.

With reference to Fig. 10, there is shown a 1-order chopper-stabilized sigma-delta ADC structure bk42 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the chopper-stabilized sigma-delta ADC structure bk18 of the present invention shown in Fig. 3(a). Fig. 11 shows a single-input-to-single-output 1-order one-bit chopper-stabilized sigma-delta ADC circuit ck8 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure bk42 of Fig. 10. The blocks bk39, bk40, and bk41 in the structure bk42 of Fig. 10 correspond to the circuit blocks ck5, ck6, and ck7 in the circuit ck8 of Fig. 11, respectively. The building block bk34 in the structure bk42 of Fig. 10 may be implemented by the circuit ck25 shown in Fig. 5(c). the block bk39 may be implemented by using the blocks 11 and 12 to control the differential signals, as shown in Fig. 11. The block bk41 may be implemented by using the clocks 11 and 12 to control the positive logic (Q) and negative logic (Q) of the comparator cp2, as shown in Fig. 11.

With reference to Fig. 12, there is shown a 2-order chopper-stabilized sigma-delta ADC structure bk57 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the chopper-stabilized sigma-delta ADC structure bk9 of the present invention shown in Fig. 2. Fig. 13 shows a fully-

differential 2-order one-bit chopper-stabilized single-delta ADC circuit ck12 with $Z^{-1}/(1+Z^{-1})$ as building block, designed on the basis of the structure bk57 of Fig. 12. The blocks bk54, bk55, and bk56 in the structure bk57 of Fig. 12 correspond to the circuit blocks ck9, ck10, and ck11 in the circuit ck12 of Fig. 13, respectively. The building blocks bk46 and bk49 in the structure bk57 of Fig. 12 may be implemented by the circuit ck26 shown in Fig. 6(b). The block bk54 may be implemented by using the clocks 11 and 12 to control the differential signals, as shown in Fig. 13. The block bk56 may be implemented by using the clocks 11 and 12 to control the positive logic(Q) and negative logic ($\overline{Q}$) of the comparator cp3, as shown in Fig. 13.

Of course, a variety of structures and circuits in addition to the above-described examples may be designed on the basis of the chopper-stabilized sigma-delta ADC structure bk9 or bk18 of the present invention. For example, the single-input-to-single-output 2-order one-bit chopper-stabilized sigma-delta ADC with $Z^{-1}/(1+Z^{-1})$ as building blocks; the fully-differential 1-order one-bit chopper-stabilized sigma-delta ADC with $(1-Z^{-1})$ as building block; the fully-differential 2-order one-bit chopper-stabilized sigma-delta ADC with $(1-Z^{-1})$ as building block; the fully-differential 2-order one-bit chopper-stabilized sigma-delta ADC with $(1+Z^{-1})$ as building block, and so on. It should be understood that the gain of the circuits of the

present invention may be adjusted depending on the application requirements.

In order to verify the advantages of the present invention in removing the circuit low-frequency noises and increasing the resolution of the converter, there are described hereinafter the simulation comparisons between the conventional circuits shown in Figs. 15 and 17, and the circuits of the present invention shown in Figs. 18 and 19.

The circuit of Fig. 15 is designed from the conventional 1-order sigma-delta ADC structure of Fig. 14. An equivalent noise voltage source e1 needed by the simulation is added in front of the operational amplifier a1 shown in Fig. 15, and the simulation is achieved by use of the switched-capacitor circuit simulator software SWICAP2 developed by K. Suyama and S. C. Fang of Columbia University, U.S.A. The input signal is a sinusoidal wave with the frequency 10kHz, and the sampling frequency is 1024 KHz. There are 4096 output signals sampled for spectrum analysis. When the noise source e1 equals to zero, i.e. in a noise free condition, the simulation result is plotted in Fig. 20(a) in solid line. When the noise source e1 is a 1 kHz sinusoidal wave, i.e. in a noisy condition, the simulation result is plotted in Fig. 20(a) in phantom line. It can be clearly seen from Fig. 20(a) that the output signal is contaminated by the low-frequency noise. Fig. 18 is similar to Fig. 9, but an equivalent noise voltage source e1 is added in front of the operational amplifier a4. Using

the same parameters and conditions as above, the simulation results are plotted in Fig. 20(b). It can be clearly seen from Fig. 20(b) that the simulation results are almost the same in both noise free and noisy conditions. Therefore, the immunity from the contamination of the low-frequency noise is verified in the circuit of the present invention.

The circuit of Fig. 17 is designed from the conventional 2-order sigma-delta ADC structure of Fig. 16. Two equivalent noise voltage sources e1 and e2 needed by the simulation are added respectively in front of the operational amplifiers a2 and a3 shown in Fig. 17, and the simulation is achieved also be use of the switched-capacitor circuit simulator software SWICAP2. The input signal is a sinusoidal wave with the frequency 10 kHz, and the sampling frequency is 1024 kHz. There are 4096 output signals sampled for spectrum analysis. When both of the noise sources e1 and e2 equal to zero, i.e. in a noise free condition, the simulation result is plotted in Fig. 21(a) in solid line. When the noise source e1 is a 1 kHz sinusoidal wave, and the noise source e2 is a 4kHz sinusoidal wave, i.e. in s noisy condition, the simulation result is plotted in Fig. 21(a) in phantom line. It can be clearly seen from Fig. 21(a) that the output signal is contaminated by the low-frequency noise. Fig. 19 is similar to Fig. 13, but two equivalent noise voltage sources e1 nd e2 are added respectively in fronts of the operational amplifiers a5 and a6. Using the same parameters and conditions as above, the

simulation results are plotted in Fig. 21(b). It can be clearly seen from Fig. 21(b) that the simulation results are almost the same in both of noise free condition and noisy condition. Therefore, the immunity from the contamination of the low-frequency noise is verified again in the circuit of the present invention.

It has been verified from both theoretical derivation and computer simulation that the present invention is immune from the low-frequency noise, so that the resolution of the sigma-delta ADC can be greatly increased. Thus, the present invention is very suitable to be applied to the high-resolution($\geq$ 16 bits) sigma-delta analog-to-digital converter circuits.

While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention need not be limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A chopper-stabilized sigma-delta analog-to-digital converter (ADC) comprising:

a first discrete-time multiplier adapted to receive an analog input signal and a first discrete-time sequence, and to multiply said analog input signal by said first discrete-time sequence to produce a choppered analog signal; and

a chopper sigma-delta analog-to-digital converter (ADC) connected in series to said first discrete-time multiplier in order to receive and convert said choppered analog signal into a digital output signal, said chopper sigma-delta ADC being characterized in z-domain by:

$$Y'(z)=X'(z)\ ST'(z) + Q(z)NT'(z),\ z= e^{jw}$$

wherein ST'(z) is a signal transfer function, and is characterized by having a passband in a high-frequency range; and NT'(z) is a noise transfer function, and characterized by having a high attenuation is said high-frequency range.

2. A chopper-stabilized sigma-delta ADC as claimed in claim 1, wherein said fist discrete-time sequence is consisted of alternating "1" and "-1" digital signals.

3. A chopper-stabilized sigma-delta ADC as claimed in claim 1, wherein said first discrete-time sequence is consisted of alternating "1" and "0" digital signals.

4. A chopper-stabilized sigma-delta ADC as claimed in claim 2, further comprising a second discrete-time multiplier connected in series to said chopper sigma-delta ADC in order to receive said digital output signal, said second discrete-time multiplier adapted to receive a second discrete-time sequence, and multiplying said digital output signal by said second discrete-time sequence to produce a choppered digital signal.

5. A chopper-stabilized sigma-delta ADC as claimed in claim 4, wherein said second discrete-time sequence is consisted of alternating "1" and "-1" digital signals.

6. A chopper-stabilized sigma-delta ADC as claimed in claim 5, wherein said high-frequency range is an area around an angular frequency π.

7. A chopper-stabilized sigma-delta ADC as claimed in claim 3, further comprising a second discrete-time multiplier connected in series to said chopper sigma-delta ADC in order to receive said digital output signal, said second discrete-time multiplier adapted to receive a second discrete-time sequence, and multiplying said digital output signal by said second discrete-time sequence to produce a choppered digital signal.

8. A chopper-stabilized sigma-delta ADC as claimed in claim 7, wherein said second discrete-time sequence is consisted of alternating "1" and "-1" digital signals.

9. A chopper-stabilized sigma-delta ADC as claimed in claim 8, wherein said high-frequency range is an area around an angular frequency π.

10. A chopper-stablised sigma-delta analogue-to-digital converter substantially in accordance with any embodiment hereinbefore described with reference to Figures 2a to 4, 5c, 6b, 7b to 13 and 18 to 21(b) of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

26

Application number

GB 9310144.2

Relevant Technical fields

(i) UK Cl (Edition L) H3H (HAH)

(ii) Int Cl (Edition 5) H03M

Search Examiner

J DONALDSON

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI, INSPEC

Date of Search

16 JUNE 1993

Documents considered relevant following a search in respect of claims 1-10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	US 5179380 (WHITE) see column 1, line 1 - column 2, line 64	1,2

Category	Identity of document and relevant passages 27	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

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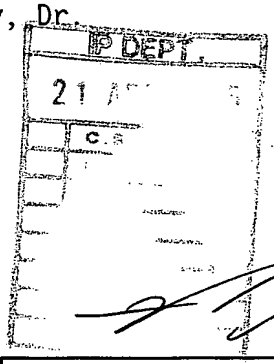

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Datum/Date
21.04.05

Zeichen/Ref./Réf.	Anmeldung Nr./Application No./Demande n°./Patent Nr./Patent No./Brevet n°.
U.KOC 3-1	05250868.6-2206-

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire
LUCENT TECHNOLOGIES INC.

COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

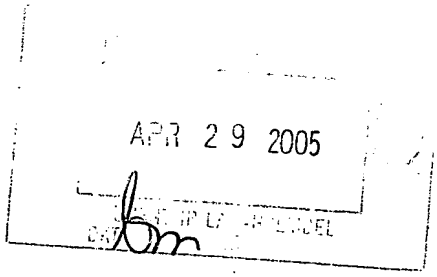
☐ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

The following specifications given by the applicant have been approved by the Search Division:

☒ abstract ☒ title

☐ The abstract was modified by the Search Division and the definitive text is attached to this communication.

The following figure will be published together with the abstract: 2



REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 05 25 0868

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X A	US 6 459 743 B1 (LIPKA DIETMAR) 1 October 2002 (2002-10-01) * column 3, line 48 - column 6, line 15 * * column 8, line 49 - column 9, line 45; figures 1-3,6 *	1-5,710 6	H03M1/12 H03H17/04
A	US 6 693 573 B1 (LINDER LLOYD) 17 February 2004 (2004-02-17) * column 3, line 13 - column 5, line 65 * * column 9, lines 10-29; figures 1,3 *	1-10	
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H03M
H03H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	13 April 2005	Waters, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
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EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 05 25 0868

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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